

A close-up photograph of a computer motherboard. The image shows a CPU with its gold pins, various capacitors labeled C107, C108, C112, and C113, and other components. The motherboard is green with white circuit traces. The text "MB120 DS SERVICE MANUAL" is overlaid on the right side of the image.

MB120 DS

SERVICE MANUAL

Table of Contents

1. INTRODUCTION	2
2. MICROCONTROLLER (MSTAR MSD95M0D).....	3
3. VIDEO BACK-END PROCESSOR (MSTAR)	10
MST7410FE	10
4. AUDIO AMPLIFIER STAGES	13
A. MAIN AMPLIFIER (U8) (10W/12W options)	13
B. HEADPHONE AMPLIFIER (U59).....	15
C. SUBWOOFER PREAMPLIFIER (U30).....	16
5. POWER STAGE.....	17
A. TPS54528	18
B. TPS54628	20
C. TPS54821	22
D. TPS563200	24
E. FDS4685.....	26
F. NTGS3446.....	27
G. APL5910.....	28
H. APL2111H.....	30
6. 2Gb DDR3 SDRAM	32
Hynix H5TQ2G63GFR.....	32
7. 4Gb DDR3L SDRAM.....	33
Hynix H5TQ4G63GFR.....	33
8. 32GBIT (4G X 8 BIT) NAND FLASH MEMORY.....	35
MT29F4G08ABAEAWP	35
9. 16M-BIT [16M x 1] CMOS SERIAL FLASH EEPROM.....	37
A. MX25L1606E SPI Flash	37
B. M25Q32FV SPI Flash.....	39
10. STDP4320 (DP1.2 splitter IC).....	41
11. ep9162s & EPF025r (HDMI 2.0a / HDCP2.2 Splitter IC).....	43
12. OPS - OPEN PLUGGABLE SPECIFICATION(OPtional)	46
13. TUNER (Optional).....	50
M88TS2022 Satellite Tuner	50
14. DEMODULATOR STAGE (Optional).....	52
15. LNB SUPPLY AND CONTROL IC (Optional).....	55
TPS65233.....	55
16. bq32000 rtc Real-Time Clock (Optional).....	56
17. SOFTWARE UPDATE.....	57

A. Main SW update	57
B. Displayport fw update	57
C. HDMI SPLITTER FW UPDATE.....	57
18. TROUBLESHOOTING	58
A. No Backlight Problem.....	58
B. Staying in Stand-by Mode	61
C. IR Problem.....	62
D. Keypad Touchpad Problems	63
E. USB Problems.....	64
F. No Sound Problem	65
G. Standby On/Off Problem.....	65
H. No Signal Problem	65
I. Real time clock problem.....	67
19. GENERAL BLOCK DIAGRAM	68

1. INTRODUCTION

17MB120DS main board is driven by MStar SOC. This IC is a single chip iDTV solution that supports channel decoding, MPEG decoding, and media-center functionality enabled by a high performance AV CODEC and CPU. This IC also supports 4K2K (UHD).

Key features includes:

- Combo Front-End Demodulator
- A multi standart A/V format decoder
- The MACEpro video processor
- Home theatre sound processor
- Internet and Variety of Connectivity Support
- Dual-stream decoder for 3D contents
- Multi-purpose CPU for OS and multimedia
- Peripheral and power management

Supported peripherals are:

- HDCP 2.2 / HDMI1.4 (FHD) input (1 HDMI default, 1 HDMI opt. with DVI, 1 HDMI opt. with OPS)
- HDCP 2.2 / HDMI2.0 (UHD) input (1 HDMI default, 1 HDMI opt. with DVI, 1 HDMI opt. with OPS)
- 1 Displayport1.2a input / 1 DP 1.2a output
- 1 PC (VGA) input
- 1 YPbPr / Back S-Video
- Line In/ Line out
- 1 Optic S/PDIF output
- 1 USB 3.0, 1 USB 2.0 port
- 1 USB2.0 for touchscreen (optional)
- 1 OPS interface (optional)
- 1 Extender IR

- 1 Dsub9 RS232
- 1 RJ45 10/100 Support Ethernet
- 1 RJ12 (for service only)
- Tuner ATV/DVB-T/T2/C (optional)
- 4K2K@ 50/100Hz Vby1, FHD@ 50/100Hz LVDS interface

2. MICROCONTROLLER (MSTAR MSD95M0D)

General Description

The MSD95M0D is MStar's most up-to-date system-on-chip solution for flat panel integrated digital television products. Building on the success of MStar's advanced technologies, the MSD95M0D hosts the most advanced picture processing engine, MStarACE-PRO3^{UC}, for all the experts in various of TV video quality tuning fields to develop the state-of-the-art DTV system. The powerful CPUs and GPUs deliver high performance for modern Linux and Android TVs. The popular ARM and Mali architecture ensures the best software compatibility. Applications with HTML5, Java, Flash, etc., can be realized on MSD95M0D with minimized developer efforts.

MACE-PRO3^{UC}, the Professional UC Edition of MStar video processor, includes all MStar's successful color-tuning tools and a newly added multi-dimensional color/sharpening/NR formula that can quickly reflect subtle or sudden changes in even darker, brighter, or mixture scenes. With this ultimate color processor, a specially designed color remapping system for modern wide gamut displays, and an easy-to-use color-tool UI, developers can quickly and easily identify PQ characteristic from the most high-end panel models to the most conventional panel models. MStar's innovated UltraClear DTV video processor adopts multi-frame video recovery technology to perfectly restore the contents/details, and eliminate the noise/artifacts from broadcasting or Internet videos.

The MSD95M0D also integrates all-purpose AV decoders for DTV/multi-media applications, ATSC/QAM, DVB-T, DVB-C, ISDB-T, DTMB Demodulator and Sound/Video processors into a single device. This allows the overall BOM to be reduced significantly and making the MSD95M0D a very cost effective multi-standard DTV solution.

The MSD95M0D enables feature rich products that bring differentiation to the iDTV market. By the use of powerful CPU/GPU and AV decoders capable of decoding a plethora of high definition content from Ethernet, USB 3.0 connectivity and MHL. The MSD95M0D based systems can provide a high quality media-center experience.

The MSD95M0D provides legacy multi-standard analog TV support with adaptive 3D video decoding and VBI data extraction. Similarly the audio decoder is capable of decoding FM, AM, NICAM, A2, BTSC and sound standards.

The MSD95M0D supplies all the necessary A/V inputs and outputs to complete a receiver design including a multi-port HDMI receiver and component video ADC. All input selections multiplexed for video and audio are integrated, including full SCART supported with CVBS output.

To meet the increasingly popular energy legislative requirements without the use of additional hardware, MSD95M0D has an ultra low power standby mode during which an embedded MCU can act upon standby events and wake up the system as required.

Features

MSD95M0D is a highly integrated smart TV solution which supports dual channel 8/10bit LVDS output, DTV channel decoding, MPEG decoding, VP decoding, 3D formatter, and security OS. MSD95M0D serves full functions of multi-media centers with a high performance CPU, GPU, and AV CODEC/security engines.

Key features includes:

1. ATSC/ISDB-T/DVB-C/DVB-T/DTMB Front-End Demodulators
 2. Advanced Multi-Core CPU and 3D GPU
 3. 3D Formatter Engine
 4. Multi-Standard A/V Format Decoder
 5. The MACE-PRO3^{LC} Video Processor
 6. Home Theater Sound Processor
 7. Internet and Variety of Connectivity Support
 8. Peripheral and Power Management
 9. Robust and Efficient Security Engine
 10. Full Multi-Media Decoders Including HEVC Decoder Supporting up to UHD/60fps Resolution
- High Performance Micro-processor
 - ARM Advanced Multi-Core CPU
 - 32KB/32KB I/D cache
 - 256KB L2 cache
 - Supports Neon instruction sets
 - 3D Graphic GPU
 - ARM Advanced Multi-Core GPU
 - Supports OpenGL ES 1.1/2.0
 - Supports OpenGL VG 1.1
 - Supports rendering size up to UHD
 - Transport Stream De-multiplexer
 - Supports three parallel TS interfaces, with or without sync signal
 - Supports two programmable TS input/output for external CI module
 - Supports external demodulators
 - TS data rate is 120Mbit/s for serial and 24MByte/s for parallel
 - 128 general purpose PID filters and 128 section filters for all transport stream de-multiplexer
 - Supports additional audio/video/PCR filters
 - Supports TS DMA channel for time-shift
 - Supports 3DES/DES and AES encryption/decryption
 - MPEG-2 Video Decoder
 - ISO/IEC 11172-2 MPEG-1 video format decoding
 - ISO/IEC 13818-2 MPEG-2 video MP@HL and HD level
 - Supports resolution up to HDTV (1080p, 1080i, 720p) and SDTV
 - Supports dual stream decoding for 3D content
 - MPEG-4 Video Decoder
 - ISO/IEC 14496-2 MPEG-4 ASP video decoding up to HD level
 - Supports resolutions up to HDTV (1080p@30fps)
 - Supports DivX Home Theater & HD profiles
 - Supports FLV version1 video format decoding
 - Supports dual stream decoding for 3D content
 - H.264 Decoder
 - ITU-T H.264, ISO/IEC 14496-10 (main and high profile up to level 5.0) video decoding
 - Supports resolution up to 4096x2160@30fps
 - Supports bitrate up to 135Mbps, the upper limit of level 5
 - Supports resolutions for all DVB, ATSC, HDTV, DVD and VCD
 - Supports SVAE 2ES (for Dual Decode)
 - Supports MVC 3D decoding upto 1080p@60fps
 - H.264 MVC Decoder
 - ITU-T H.264, ISO/IEC 14496-10 video decoding (Main and high profile up to level 4.2)
 - Supports resolution up to 1080p@60fps

- **VP8 Decoder** Optional
 - Supports Google VP8 decoder
 - Supports resolution up to 1920x1080@60p
 - Supports maximum bitrate upto 50Mbps
- **VP9 Decoder**
 - Supports Google VP9 decoder
 - Supports 4:2:0 subsampling and 8bit/10bit color depth
 - Supports max resolution and frame rate 4096x2160@60fps
 - Supports max bitrate upto 100Mbps
- **AVS+ Decoder** Optional
 - Supports Broadcasting profile, level 6.0.1.08.60 (AVS+)
 - Supports Jizhun profile, level 6.0
 - Supports bitrate up to 50Mbps
 - Supports resolution up to 1920x1080@60fps
 - Supports dual stream decoding
- **RealMedia Decoder** Optional
 - Supports RV8, RV9, RV10 decoders
 - Supports file formats with RM and RMVB
 - Supports maximum resolution up to 1080p@60fps
 - Supports Picture Re-sampling
 - Supports in-loop de-block for B-frame
 - Supports dual stream decoding
- **HEVC (H.265) Decoder**
 - Supports HEVC/H.265 video decoding.
 - Supports Main/Main-10 profile, level 5.1, high tier
 - Supports 8-bit/10-bit color depth
 - Supports resolution up to 4096x2160@60fps
 - Supports max bitrate upto 160 Mbps
- **H.264 Encoder**
 - Supports H.264 encoding, Main Profile, level 4.1
 - Maximum output frame-rate/resolution: 1920x1080@30fps, 1280x720@60fps
 - Supports MVs: 16x16, 16x8, 8x16, 8x4, 4x8, 4x4
 - Supports up to quarter-pel
 - Supports up to two reference frames
- **Hardware PNG / GIF Decoder**
 - Supports up to 8192 x 8192 (per channel 8 bits), or 4096 x 8192(per channel 16 bits) pixel image
 - PNG format 1bpp/2bpp/4bpp/8bpp index(palette) mode support
 - PNG transparency mode support
 - interlaced / non-interlaced GIF support
 - ARGB8888, RGB565, YUV422(YUYV),YUV422(YVYU),gray, gray with alpha output format support
- **Hardware JPEG Decoder**
 - Supports upto 1920x1080@30p, 1280x720@60p
 - Supports formats: 422/411/420/444/422T
 - Supports scaling down ratios: 1/2x1/2, 1/4x1/4, 1/8x1/8
 - Supports both color and grayscale pictures
 - Supports sequential mode, single scan
 - Supports programmable Region of Interest (ROI)
 - Following the file header scan the hardware decoder fully handles the decode process
- **VC-1 Video Decoder** Optional
 - Supports SMPTE-421 (WMV video) decoding up to MH@HL
 - Supports SMPTE-421 (VC1 video) decoding up to AP@L3
 - Supports dual stream decoding for 3D content
- **NTSC/PAL/SECAM Video Decoder**
 - Supports NTSC-M, NTSC-J, NTSC-4.43, PAL (B, D, G, H, M, N, I, Nc), and SECAM standards
 - Automatic standard detection
 - Motion adaptive 3D comb filter
 - Three configurable CVBS & Y/C S-video inputs
 - Supports Teletext, Closed Caption (analog CC 608/ analog CC 708) and V-chip
- **Multi-Standard TV Sound Processor**
 - Supports BTSC/A2 demodulation
 - Supports NICAM/FM/AM demodulation
 - Supports MTS Mode Mono/Stereo/SAP in BTSC mode
 - Supports Mono/Stereo/Dual in A2/NICAM mode
 - Built-in audio sampling rate conversion (SRC)

- Audio processing for loudspeaker channel, including volume, balance, mute, tone, EQ, virtual stereo/surround and treble/bass controls
- Advanced sound processing options available, for example: Dolby¹, DTS³
- Supports digital audio format decoding:
 - MPEG-1, MPEG-2 (Layer I/II), MP3, Dolby Digital (AC-3)^{Optional}, AAC-LC, HE-AAC, WMA, and WMA9 Pro
 - Supports^{2Optional} Dolby Digital Plus, Dolby Pulse, and MS11/MS12 multistream decoder, including Dolby Digital Encoder for transcoding streams to Dolby Digital 5.1(DDCO), DTS M6 multistream decoder/encoder
- Supports Audio Description
- Supports MPEG audio encoding
- Supports time-shifting PVR
- Supports programmable delay for audio/video synchronization
- **Audio Interface**
 - Three L/R audio line-inputs including two mono Mic. Inputs
 - One L/R outputs for main speakers, monitor output, and SCART output
 - Supports stereo headphone driver
 - I2S digital audio output
 - S/PDIF digital audio output and input
 - Support HDMI receiver ARC function
- **Analog RGB Compliant Input Ports**
 - Three analog ports support up to 1080P
 - Supports PC RGB input up to SXGA@75Hz
 - Supports HDTV RGB/YCbPr/YCbCr
 - Supports Composite Sync and SOG Sync-on-Green
 - Automatic color calibration
- **Analogue RGB Auto-Configuration & Detection**
 - Auto input signal format and mode detection
 - Auto-tuning function including phasing, positioning, offset and gain configuration
 - Sync Detection for H/V Sync
- **DVI/HDCP/HDMI/MHL Compliant Input Ports**
 - Four HDMI/DVI Input port
 - HDMI 2.0/1.4b Compliant
 - MStar iSwitch for fast HDMI switching
 - HDCP 2.2/1.4 Compliant
 - Support embedded HDCP 1.4 Key
 - Support external HDCP 2.2 key
 - Supports HDMI CEC
 - Supports HDMI 3D formats
 - Supports HDMI ARC
 - Robust receiver with excellent long-cable support
- **MHL Input Ports**
 - One MHL Input port (combo with HDMI/DVI)
 - MHL 3.0/2.1 compliant
- **MStar Advanced Color Engine - Professional UC Edition (MACE-PRO3^{UC})**
 - 10/12-bit internal Data Processing
 - Support up to 4k@60p
 - Dual-Engine Architecture supporting PIP/PBP
 - MACE-PRO4UC Advanced Scaling Engine:
 - Multi-directional Scaling Technology
 - High-Tap Filters with Programmable Parameter
 - De-jagging Support
 - Video Feather Artifact Detection and Removal
 - Nonlinear Video Scaling
 - Dynamic Scaling for RM, VC-1^{Optional}
 - Native resolution reappear
 - Nonnative detail generator
 - Content-Aware sharpness enhancements
 - MACE-PRO3UC DTV Video Processing Technology:
 - UltraClear-PRO3 Video Deinterlacing with Motion Object Stabilizer
 - Edge-Oriented Deinterlacer with Edge Smoothing and Artifact Removal
 - Automatic 3:2/2:2/M:N Pull-Down Detection and Recovery
 - UltraClear-PRO3 Noise Reduction
 - Video Detection & Repairing Technology for Lousy Inputs such as Internet Streaming

- MACE^{LIVE}-PRO Color Engine with Accurate Color Tuning Support
- Cross-Color Suppression Support
- Supports Hanging Dot Search & Removal
- UltraClear-Based De-Flickering
- MPEG Artifact Removal Including Blocking and Mosquito Noise Cancellation
- Arbitrary Frame Rate Conversion
- MACE-PRO3UC Picture Enhancement:
 - Enhancements in All Features of MACE-3/4 Engine
 - Super Resolution for Detail Enhancement & Recovery
 - Scene Detection
 - 3D Adaptive Color Control
 - 3D Adaptive Sharpness Control
 - sRGB and xvYCC Color Processing Engine
 - Supports HDMI 1.4 Deep Color Format
 - Supports HDMI 1.4 sYCC601 / AdobeRGB / AdobeYCC601 Color Formats
 - Supports Enhanced and Seamless Color Mapping for Wide Gamut Panels
- Programmable 12-bit RGB gamma CLUT
- Top/Bottom, Left-Right 3D Format Auto-Detection
- Supports 2D to 3D conversion
- **Output Interface**
 - Single/Dual link 8/10-bit LVDS output
 - 8 lane 8/10-bit Vby1 output (configurable width: 2/4/8 lane)
 - Supports panel resolution up to Full HD 1920x1080@ 60Hz (LVDS 2ch)
 - Supports panel resolution up to Ultra HD @ 60Hz (Vby1 8 lane)
 - Supports dithering options
 - Supports OSD bypass to MStar FRC 120Hz/240Hz chip (optional)
 - Spread spectrum output frequency for EMI suppression
 - Supports direct and edge types local dimming
 - Supports 60Hz 3D polarized panel (line interleave)
 - Supports Cinema output mode
- **CVBS Video Encoder**
 - Supports all NTSC/PAL TV Standard
 - Stand-alone scaling engine (no vertical scaling up)
 - Programmable Hue, Contrast, Brightness
 - Supports TTX/CC/WSS output
- **CVBS Video Output**
 - Allows CVBS output of digital content to SCART
- **2D Graphics Engine**
 - Hardware Graphics Engine for responsive interactive applications
 - Supports point draw, line draw, rectangle draw/fill and text draw
 - Supports BitBlt, stretch BitBlt, italic BitBlt, Mirror BitBlt and rotate BitBlt
 - Supports alpha-blending operation
 - Supports source/destination color key and alpha key
 - Supports dither
 - Supports color format conversion and format transformation
 - Raster Operation (ROP)
 - Support DFB and Porter-Duff operation
- **VIF Demodulator**
 - Compliant with NTSC M/N, PAL B, G/H, I, D/K, SECAM L/L' standards.
 - Support low IF architecture
 - Audio/Video internal dual-path processor
 - Locking range improvement
- **ATSC/QAM Demodulator**
 - ATSC A/53 compliant 8VSB
 - ITU-T J.83 Annex B, SCTE DVS-031 compliant 64/256QAM receiver
 - 2010 - A74 compliant
 - All digital demodulation and timing recovery loops for tracking frequency and clock offset
 - Automatic co-channel and adjacent channel interference suppression
 - Impulse-Noise suppression
 - Integrated deinterleaver RAM for Level 1 J = 1 and Level 2 J = 1,2,3,4
 - Supports LIF interfaces
 - I2C repeater for tuner control from backend host controller

■ ISDB-T Demodulator

- Compliant with ISDB-T ARIB STD-B31
- Compliant with ISDB-Tsb ARIB STD-B29
- Supports all modes defined in ISDB-T spec
- Supports all guard ratios: 1/4, 1/8, 1/16, 1/32
- 42ms/channel, excluding AGC time and PLL sync
- Support ZIF/LIF interfaces
- I2C repeater for tuner control from backend host controller
- Impulse-noise suppression
- Phase noise compensation

■ DVB-C Demodulator

- ITU J.83 Annex A/C DVB-C (EN 300 429) compliant
- Supports 1-7.2 M Baud symbol rate
- Automatic blind channel scan (constellation and symbol rate)
- Supports LIF interfaces
- IIS performance improvement

■ DVB-T Demodulator

- Compliant with DVB-T (ETSI EN 300 744)
- NORDIG 2.2.2, D-book 7.0 compliant
- Accept low IF inputs in 6, 7, 8MHz channel bandwidths
- Supports all guard intervals (1/32 to 1/4)
- Supports all constellations (QPSK, 16-QAM, 64-QAM)
- Ultra fast automatic blind UHF/VHF channel scan
- Optimized for SFN channels with pre/post-cursive echoes inside/outside the guard
- Phase-Noise suppression
- Impulse-Noise suppression
- All digital demodulation and timing recovery loops for tracking frequency and clock offset
- Automatic co-channel and adjacent channel interference suppression
- CNR performance improvement

■ DTMB Demodulator

- Compliant with DTMB GB 20600-2006
- Compliant with DTMB GB/T 26686-2015
- Support all valid combinations of FH mode, modulation, code rate and interleaving mode
- Support LIF interfaces
- Automatic co-channel and adjacent channel interference suppression
- CCI and ACI rejection capability
- Impulse-noise suppression

■ Connectivity

- Four USB 2.0 host ports
- One USB 3.0 host ports
- USB architecture designed for efficient support of external storage devices in conjunction with off air broadcasting
- USB port supports efficient battery charger
- Embedded 10/100 Ethernet MAC and PHY
- Support Ethernet Wake-On-Lan

■ Miscellaneous

- DRAM interface dual channel, 32bit x 2 DRAM bus up to four 16-bit DDR3
- Supports PVR
- Supports Common Interface for conditional access support
- Bootable SPI interface with serial flash support
- Parallel interface for external parallel eMMC flash (optional) and NAND flash support
- Power control module with ultra low power MCU available in standby mode
- 931-ball BGA package
- Operating Voltages: 1.5V (DDR3), 1.8V (eMMC), and 3.3V (I/O and analog)

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
3.3V Supply Voltages	V_{VDD_33}	3.14		3.46	V
1.8V Supply Voltages	V_{VDD_15}	1.43		1.57	V
Core Supply	V_{VDD_core}		0.95		V
Ambient Operating Temperature	T_A	0		70	°C
Junction Temperature	T_J			125	°C

Table 1: Recommended operating conditions.

Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit
3.3V Supply Voltages	V_{VDD_33}		3.63	V
1.8V Supply Voltages	V_{VDD_15}		1.65	V
Core Supply Voltages	V_{VDD_core}		1.26	V
Input Voltage (5V tolerant inputs)	$V_{IN5Vtol}$		5.3	V
Input Voltage (non 5V tolerant inputs)	V_{IN}		V_{VDD_33}	V
Storage Temperature	T_{STG}	-40	150	°C
Junction Temperature	T_J		150	°C

Note: Stresses above those listed in Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and does not imply functional operation of the device. Exposure to absolute maximum ratings for extended periods may affect device reliability.

Table 2: Absolute Maximum Ratings

3. VIDEO BACK-END PROCESSOR (MSTAR)

MST7410FE

General Description

The MST7410FE is a highly integrated ASIC for doubling the frame rate of the video input to provide a conversion from 50Hz to 100Hz or 60Hz to 120Hz. The MST7410FE comprises LVDS/V-By-One receiver, film source detection and inversion, motion frame rate conversion, color space conversion and management.

With HS-LVDS technology, the MST7410FE can support up to 2-channel input video source which can support up to FHD 60Hz. With 12-lane V-By-One technology, the MST7410FE can support up to 8-lane input video source which can support up to QFHD 60Hz. It can also support up to 4-lane V-By-One input OSD source which can support up to QFHD 30Hz. With HDMI 2.0 technology, the MST7410FE can support up to QFHD 60Hz video source.

MACE-PRO4^{UC}, the Professional UC Edition of MStar video processor, includes all MStar's successful color-tuning tools and a newly added multi-dimensional color/sharpening/NR formula that can quickly reflect subtle or sudden changes in even darker, brighter, or mixture scenes. With this ultimate color processor, a specially designed color remapping system for modern wide gamut displays, and an easy-to-use color-tool UI, developers can quickly and easily identify PQ characteristic from the most high-end panel models to the most conventional panel models. MStar's innovative UltraClear video processor adopts multi-frame video recovery technology to perfectly restore the contents/details, and eliminate the noise/artifacts.

By utilizing MStar 11th generation MFC technology, the MST7410FE realizes an optimum frame rate conversion to meet the output display frame rate, a wide horizontal and vertical search range for QFHD input source, and detects any cadences for best motion compensation. Moreover, the MST7410FE provides a clearer and halo-free moving picture quality without motion blur or judder. With 11th generation MFC, the MST7410FE provides a Logo and Small object detection and protection technology.

Armed with MStar Genuine3D^{PRO} 2D/3D Conversion Engine, the MST7410FE provides an idealized 3D Video quality output. Moreover, the MST7410FE provides an adjustable gain and depth tuning methodology for customized 3D effect.

For green power saving, the MST7410FE provides a local dimming control circuit. The dimming control range maximum region is 2304 . The output interface could be SPI interface or direct PWM output pin.

Parameter	Symbol	Min	Typ	Max	Units
3.3V Supply Voltages	V _{VDD 33}	3.14		3.46	V
1.5V Supply Voltages	V _{VDD 15}	1.43		1.57	V
0.95V Supply Voltages ^{Note}	V _{VDD 095}	0.9		1.05	V
Ambient Operating Temperature	T _A	0		70	°C
Junction Temperature	T _J			125	°C

Note: 0.95V supplying voltages ripple within 100mV (+/-50mV)

Table 3: Recommended operating conditions

Features

- **High Speed Input Interface**
 - Input interface selectable as:
 - 2 HS-LVDS Links up to 150MHz for F-HD @ 60Hz
 - 12 lane V-By-One up to 3.75Gbps, 8-lane for 4K2K @ 60Hz, 4-lane for 4k2k @30Hz
- **High Speed Output Interface**
 - 16 lane V-By-One up to 3.75Gbps for 4K2K @ 120Hz QFHD panel
- **HDCP/HDMI Compliant Input Ports**
 - 2 HDMI input ports and 1 HDMI output port (bypass)
 - HDMI 2.0 Compliant
 - HDCP 2.2 Compliant
 - Supports HDMI CEC
- **Memory Interface**
 - Embedded DDR3 1 Gb X4
- **11th Generation MFC Engine (FRC11)**
 - Advanced Halo Reduction plus
 - Motion Compensated Frame Rate Conversion
 - Motion Blur Elimination to improve MPRT
 - Automatic Film-Mode Detection
 - Film Judder Cancellation
 - MStar Genuine3D^{PRO} 2D/3D Conversion Engine
 - 3D Depth Control for native 3D / Converted 3D Inputs
 - Major frame rate conversion:
 - 24Hz → 120Hz
 - 25Hz → 100/120Hz
 - 30Hz → 120Hz
 - 50Hz → 100/120Hz
 - 60Hz → 120Hz
 - Multi-Cadence Conversion
 - Artificial Object Detection
 - Search range: Big H and V search range to handle fast H/W motion
 - Supports Logo detection and protection
 - Supports small object detection and protection
 - Advanced handling for small object, logo rim detection, fade in/out, flash, periodical etc.
- **Uniformity Correction Engine**
 - Block Size: 8 pixel x 8 line
 - Layer Number: 6 layers
 - Data Length: 10-bit
- **3D Formatter**
 - Supports mandatory HDMI1.4a 3D video timing
 - Supports 1080p and 720P frame pack mode handling
 - Supports Checker Board and Pixel Alternative 3D mode
 - Supports 3D format translator
 - 3D Output Support: SG/PR
 - Supports 3D Frame ID Output
- **MStar Advanced Color Engine – Professional UC Edition (MACE-PRO4^{UC})**
 - 10/12-bit internal Data Processing
 - MACE-PRO4^{UC} Advanced Scaling Engine:
 - Multi-directional Scaling Technology
 - High-Tap Filters with Programmable Parameter
 - De-jagging Support
 - Video Feather Artifact Detection and Removal
 - Native resolution reappear
 - Nonnative detail generator
 - Content-Aware sharpness enhancements
 - MACE-PRO3^{UC} Picture Enhancement:
 - Enhancements in all features of MACE-3/4 Engine
 - Super Resolution for Detail Enhancement & Recovery
 - Scene Detection
 - 3D Adaptive Color Control
 - 3D Adaptive Sharpness Control
 - sRGB and xvYCC Color Processing Engine
 - Supports HDMI 1.4 Deep Color Format
 - Supports HDMI 1.4 sYCC601 / AdobeRGB / AdobeYCC601 Color Formats
 - Supports Enhanced and Seamless Color Mapping for Wide Gamut Panels
 - Programmable 12-bit RGB gamma CLUT

■ Local Dimming Support

- Supports Direct/Edge Type Local Dimming
- Max Block number: 48X48
- Programmable Light Spread Profile

■ Miscellaneous

- Dual Core RISC CPU
- Dual Full Duplex U-ART Interface
- Two Channel SPI Interface / One I2C-M for Dimming Control
- Supports memory minor mode
- Supports 3D_SYNC output pin
- Shutter glasses control signals:
 - L/R sync signal phase, polarity, duration programmable
 - IR Sync programmable
- Supports PWM output for scan backlight control

- One I²C Master Channel and one I²C Slave Channel
- Supports built-in spread spectrum clock for reducing EMI issue
- 27x27 BGA package
- Operating Voltages: 0.95V, 1.5V and 3.3V

■ Separate OSD Data Path Support

- Max resolution support: 4K2K @ 30Hz
- Supports OSD scaling up
- Supports OSD sharpness adjust
- OSD support format:
 - Supports ARGB 1555
 - Supports ARGB 4444
 - Supports ARGB 8888
 - Supports Color Key with one programmable key value

Block Diagram

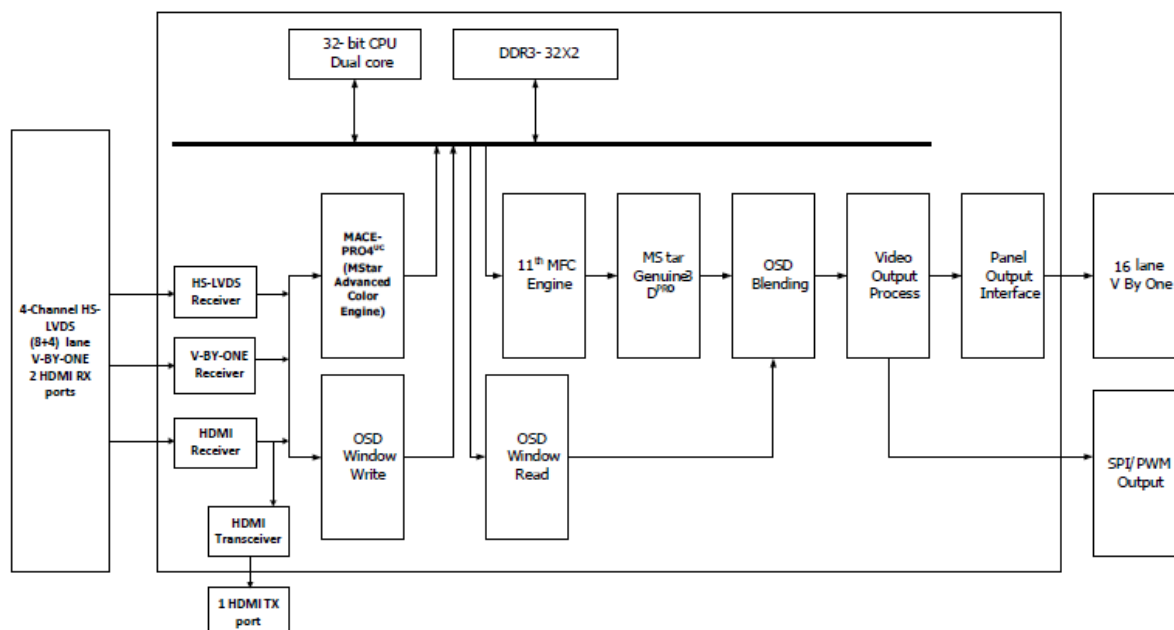


Figure 1: Block diagram

4. AUDIO AMPLIFIER STAGES

A. MAIN AMPLIFIER (U8) (10W/12W OPTIONS)

Description

AD82587D is a digital audio amplifier capable of driving a pair of 8 ohm, 20W or a single 4 ohm, 40W speaker, both which operate with play music at a 24V supply without external heat-sink or fan requirement.

Using I²C digital control interface, the user can control AD82587D's input format selection, DRC (dynamic range control), mute and volume control functions. AD82587D has many built-in protection circuits to safeguard AD82587D from connection errors.

Features

- 16/18/20/24-bit input with I²S, Left-alignment and Right-alignment data format
- PSNR & DR(A-weighting) Loudspeaker: 97dB (PSNR), 105dB (DR) @ 24V
- Multiple sampling frequencies (Fs)
 - 32kHz / 44.1kHz / 48kHz and
 - 64kHz / 88.2kHz / 96kHz and
 - 128kHz/176.4kHz/192kHz
- System clock = 64x, 128x, 256x, 384x, 512x, 768x,1024x Fs
 - 256x~1024x Fs for 32kHz / 44.1kHz / 48kHz
 - 128x~512x Fs for 64kHz / 88.2kHz / 96kHz
 - 64x~256x Fs for 128kHz /176.4kHz/192kHz
- Supply voltage
 - 3.3V for digital circuit
 - 10V~26V for loudspeaker driver
- Loudspeaker output power for Stereo@ 24V
 - 10W x 2ch into 8_ @ 0.16% THD+N
 - 15W x 2ch into 8_ @ 0.18% THD+N
 - 20W x 2ch into 8_ @ 0.24% THD+N
- Loudspeaker output power for Mono@ 24V
 - 20W x 1ch into 4_ @ 0.17% THD+N
 - 30W x 1ch into 4_ @ 0.2% THD+N
 - 40W x 1ch into 4_ @ 0.24% THD+N
- Sounds processing including:
 - Volume control (+24dB~-103dB, 0.125dB/step)
 - Dynamic range control
 - Power clipping
 - Channel mixing
 - User programmed noise gate with hysteresis window
 - DC-blocking high-pass filter
- Anti-pop design
- Short circuit and over-temperature protection
- I2C control interface with selectable device address
- Internal PLL
- LV Under-voltage shutdown and HV Under-voltage
- detection
- Power saving mode
- Dynamic temperature control

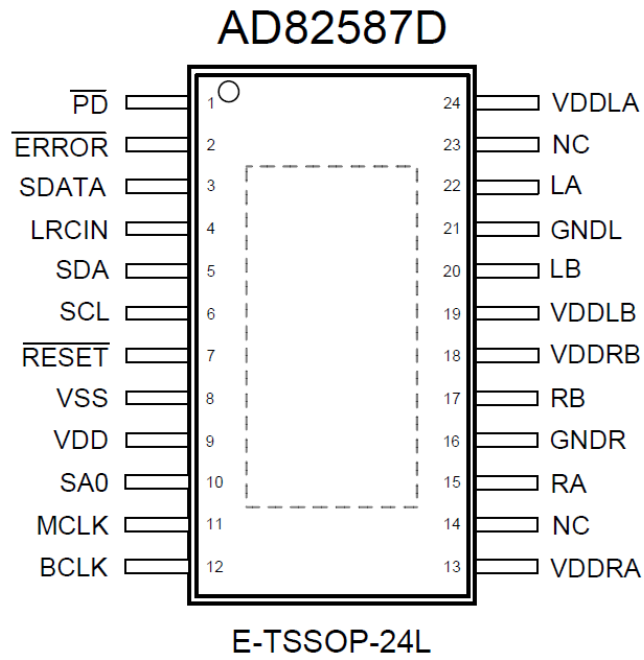


Figure 2: Pin description

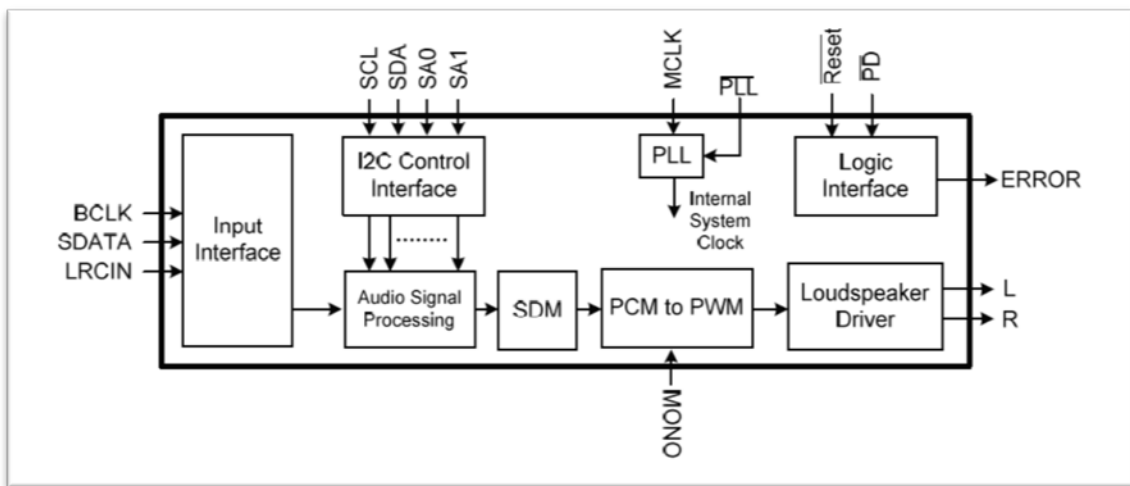


Figure 3: Functional Block Diagram

Symbol	Parameter	Min	Max	Units
DVDD	Supply for Digital Circuit	-0.3	3.6	V
VDDL/R	Supply for Driver Stage	-0.3	30	V
V_i	Input Voltage	-0.3	3.6	V
T_{stg}	Storage Temperature	-65	150	$^{\circ}\text{C}$
T_J	Junction Operating Temperature	0	150	$^{\circ}\text{C}$

Table 4: Absolute Maximum Ratings

Symbol	Parameter	Typ	Units
DVDD	Supply for Digital Circuit	3.15~3.45	V
VDDL/R	Supply for Driver Stage	10~26	V
T _J	Junction Operating Temperature	0~125	°C
T _A	Ambient Operating Temperature	0~70	°C

Table 5: Recommended Operating Conditions

B. HEADPHONE AMPLIFIER (U59)

Description

The AD22657B is a 2-Vrms cap-less stereo line driver. The device is ideal for single supply electronics. Cap-less design can eliminate output dc-blocking capacitors for better low frequency response and save cost.

The AD22657B is capable of delivering 2-Vrms output into a 10k ohm load with 3.3V supply. The gain settings can be set by users from 1V/V to 10V/V externally. The AD22657B has under voltage protection to prevent POP noise. Build-in shutdown control and de-pop control sequence also help AD22657B to be a pop-less device.

The AD22657B is available in a 10-pin MSOP package.

Features

- Operation Voltage: 3V to 3.6V
- Cap-less Output
 - Eliminates Output Capacitors
 - Improves Low Frequency Response
 - Reduces POP/Clicks
- Low Noise and THD
 - Typical SNR 107dB
 - Typical Vn 7uVrms
 - Typical THD+N < 0.02%
- Maximum Output Voltage Swing into 2.5k Load
 - 2Vrms at 3.3V Supply Voltage
- Single-ended Input
- External Gain Setting from 1V/V to 10V/V
- Fast Start-up Time: 0.5ms
- Integrated De-Pop Control
- External Under Voltage Protection
- Thermal Protection
- Less External Components Required
- +/-8kV IEC ESD Protection at line outputs

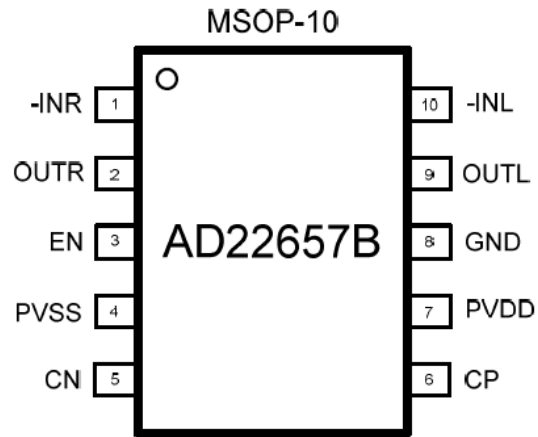


Figure 4: Pin description

No.	Name	Type ⁽¹⁾	Pin Description
1	-INR	I	Right channel OP negative input
2	OUTR	O	Right channel OP output
3	EN	I	Enable input, active high
4	PVSS	P	Supply voltage
5	CN	I/O	Charge-pump flying capacitor negative terminal
6	CP	I/O	Charge-pump flying capacitor positive terminal
7	PVDD	P	Positive supply
8	GND	P	Ground
9	OUTL	O	Left channel OP output
10	-INL	I	Left channel OP negative input

Table 6: Pin functions

SYMBOL	PARAMETER		Min	NOM	Max	UNIT
V_{DD}	Supply Voltage		3.0	3.3	3.6	V
V_{IH}	High Level Input Voltage	EN		60		% of V_{DD}
V_{IL}	Low Level Input Voltage	EN		40		% of V_{DD}
T_A	Operating Ambient Temperature Range		-40		85	°C
R_L	Load Resistance		600			Ω

Table 7: Recommended operating conditions

C. SUBWOOFER PREAMPLIFIER (U30)

AD22657B is used for subwoofer out, as well.

5. POWER STAGE

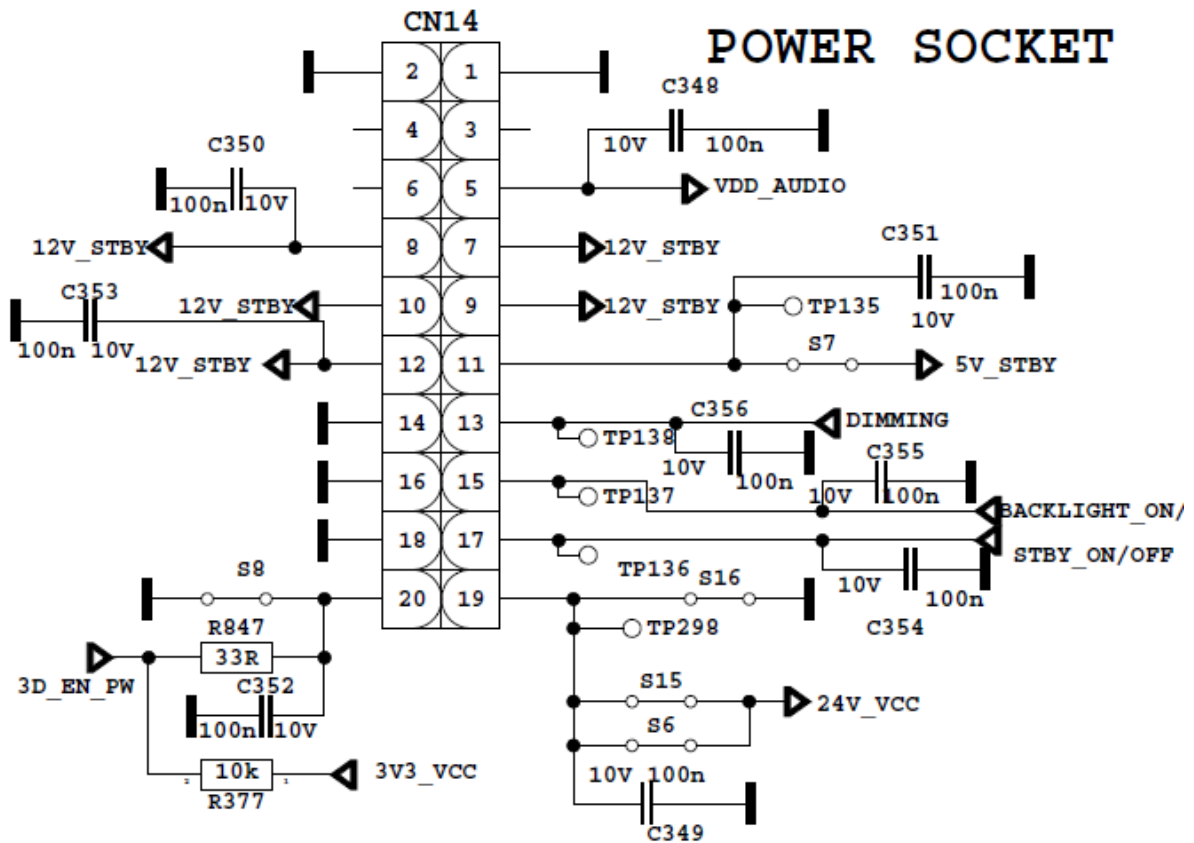


Figure 5: Power socket and options.

Power socket is used for taking voltages which are 12V, 5V and VDD_Audio. These voltages are produced in power board. Also socket is used for giving dimming, backlight and standby signals with power board. It is shown at figure 4.1.

The device operates from 4.5-V to 18-V VIN input. The output voltage can be programmed between 0.76 V and 6 V. The device also features an adjustable soft start time. The TPS54528 is available in the 8-pin DDA package, and designed to operate from -40 C to 85 C.

Features

- D-CAP2 Mode Enables Fast Transient Response
- Low Output ripple and Allows Ceramic Output Capacitor
- Wide VIN Input Voltage Range: 4.5 V to 18 V
- Output Voltage Range: 0.76 V to 6 V
- Highly Efficient Integrated FETs Optimized for Lower Duty Cycle Applications- 65 mOhm (High Side) and 36 mOhm (Low Side)
- High Efficiency, less than 10 mikroAmper at shutdown
- High Initial Bandgap Reference Accuracy
- Adjustable Soft Start
- Pre-Biased Soft Start
- 650-kHz Switching Frequency (f_{sw})
- Cycle By Cycle Over Current Limit
- Auto-Skip Eco-mode for High Efficiency at Light Load

Applications

- Wide Range of Applications for Low Voltage System
- Digital TV Power Supply
- High Definition Blu-ray Disc Players
- Networking Home Terminal
- Digital Set Top Box(STB)

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
VIN	Input operating voltage	4.5		18	V
T _J	Junction temperature	-40		125	°C

Table 8: Recommended operating conditions

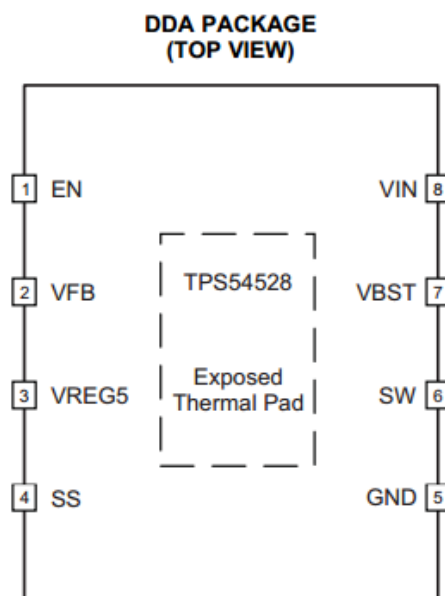


Figure 7: Pin Description

PIN		DESCRIPTION
NAME	NO.	
EN	1	Enable input control. EN is active high and must be pulled up to enable the device.
VFB	2	Converter feedback input. Connect to output voltage with feedback resistor divider.
VREG5	3	5.5 V power supply output. A capacitor (typical 1 μ F) should be connected to GND. VREG5 is not active when EN is low.
SS	4	Soft-start control. An external capacitor should be connected to GND.
GND	5	Ground pin. Power ground return for switching circuit. Connect sensitive SS and VFB returns to GND at a single point.
SW	6	Switch node connection between high-side NFET and low-side NFET.
VBST	7	Supply input for the high-side FET gate drive circuit. Connect 0.1 μ F capacitor between VBST and SW pins. An internal diode is connected between VREG5 and VBST.
VIN	8	Input voltage supply pin.
Exposed Thermal Pad	Back side	Thermal pad of the package. Must be soldered to achieve appropriate dissipation. Must be connected to GND.

Table 9: Pin functions.

B. TPS54628

General Description

The TPS54628 is an adaptive on-time D-CAP2 mode synchronous buck converter. The TPS54628 enables system designers to complete the suite of various end-equipment power bus regulators with a cost effective, low component count, low standby current solution. The main control loop for the TPS54628 uses the D-CAP2 mode control that provides a fast transient response with no external compensation components. The adaptive on-time control supports seamless transition between PWM mode at higher load conditions and Eco-mode operation at light loads. Eco-mode allows the TSP54628 to maintain high efficiency during lighter load conditions. The TPS54628 also has a proprietary circuit that enables the device to adopt to both low equivalent series resistance (ESR) output capacitors, such as POSCAP or SP-CAP, and ultra-low ESR ceramic capacitors. The device operates from 4.5-V to 18-V VIN input. The output voltage can be programmed between 0.76 V and 7 V. The device also features an adjustable soft start time. The TPS54628 is available in the 8-pin DDA and 10-pin DRC packages, and is designed to operate over the ambient temperature range of -40C to 85C.

Features

- D-CAP2 Mode Enables Fast Transient Response
- Low Output ripple and Allows Ceramic Output Capacitor
- Wide VIN Input Voltage Range: 4.5 V to 18 V
- Output Voltage Range: 0.76 V to 7 V
- Highly Efficient Integrated FETs Optimized for Lower Duty Cycle Applications- 36 mOhm (High Side) and 28 mOhm (Low Side)
- High Efficiency, less than 10 μ A at shutdown
- High Initial Bandgap Reference Accuracy
- Adjustable Soft Start
- Pre-Biased Soft Start
- 650-kHz Switching Frequency (f_{sw})
- Cycle By Cycle Over Current Limit
- Auto-Skip Eco-mode for High Efficiency at Light Load

Applications

- Wide Range of Applications for Low Voltage System
- Digital TV Power Supply
- High Definition Blu-ray Disc Players
- Networking Home Terminal
- Digital Set Top Box(STB)

over operating free-air temperature range, (unless otherwise noted)

			MIN	MAX	UNIT
V_{IN}	Supply input voltage range		4.5	18	V
V_I	Input voltage range	VBST	-0.1	24	V
		VBST (10 ns transient)	-0.1	27	
		VBST(vs SW)	-0.1	6.0	
		SS	-0.1	5.7	
		EN	-0.1	18	
		VFB	-0.1	5.5	
		SW	-1.8	18	
		SW (10 ns transient)	-3	21	
		GND	-0.1	0.1	
V_O	Output voltage range	VREG5	-0.1	5.7	V
I_O	Output Current range	I_{VREG5}	0	5	mA
T_A	Operating free-air temperature		-40	85	°C
T_J	Operating junction temperature		-40	150	°C

Table 10: Recommended operating conditions

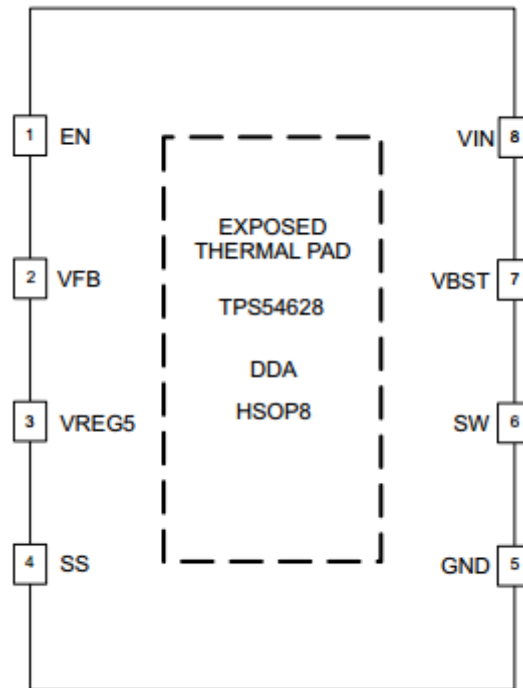


Figure 8: Pin Description

PIN FUNCTIONS

PIN		DESCRIPTION
NAME	NO.	
EN	1	Enable input control. EN is active high and must be pulled up to enable the device.
VFB	2	Converter feedback input. Connect to output voltage with feedback resistor divider.
VREG5	3	5.5 V power supply output. A capacitor (typical 1 μ F) should be connected to GND. VREG5 is not active when EN is low.
SS	4	Soft-start control. An external capacitor should be connected to GND.
GND	5	Ground pin. Power ground return for switching circuit. Connect sensitive SS and VFB returns to GND at a single point.
SW	6	Switch node connection between high-side NFET and low-side NFET.
VBST	7	Supply input for the high-side FET gate drive circuit. Connect 0.1 μ F capacitor between VBST and SW pins. An internal diode is connected between VREG5 and VBST.
VIN	8	Input voltage supply pin.
Exposed Thermal Pad	Back side	Thermal pad of the package. Must be soldered to achieve appropriate dissipation. Must be connected to GND.

Table 11: Pin functions.

C. TPS54821

General Description

The TPS54821 in thermally enhanced 3.5 mm x 3.5 mm QFN package is a full featured 17 V, 8 A synchronous step down converter which is optimized for small designs through high efficiency and integrating the high-side and low-side MOSFETs. Further space savings are achieved through current mode control, which reduces component count, and by selecting a high switching frequency, reducing the inductor's footprint. The output voltage startup ramp is controlled by the SS/TR pin which allows operation as either a stand alone power supply or in tracking situations. Power sequencing is also possible by correctly configuring the enable and the open drain power good pins. Cycle by cycle current limiting on the high-side FET protects the device in overload situations and is enhanced by a low-side sourcing current limit which prevents current runaway. There is also a low-side sinking current limit which turns off the low-side MOSFET to prevent excessive reverse current. Hiccup protection will be triggered if the overcurrent condition has persisted for longer than the preset time. Thermal hiccup protection disables the device when the die temperature exceeds the thermal shutdown temperature and enables the part again after the built-in thermal shutdown hiccup time.

Features

- Integrated 26 mΩ / 19 mΩ MOSFETs
- Split Power Rail: 1.6 V to 17 V on PVIN
- 200 kHz to 1.6 MHz Switching Frequency
- Synchronizes to External Clock
- 0.6V \pm 1% Voltage Reference Over Temperature
- Low 2 μ A Shutdown Quiescent Current
- Monotonic Start-Up into Pre-biased Outputs
- -40°C to 125°C Operating Junction Temperature Range
- Adjustable Input Undervoltage Lockout
- Adjustable Slow Start/Power Sequencing
- Power Good Output Monitor for Undervoltage and Overvoltage
- Adjustable Input Undervoltage Lockout

Applications

- Digital TV Power Supplies
- Set Top Boxes
- Blu-ray DVDs
- Home Terminals

		VALUE		UNIT
		MIN	MAX	
Input Voltage	VIN	-0.3	20	V
	PVIN	-0.3	20	
	EN	-0.3	6	
	BOOT	-0.3	27	
	VSENSE	-0.3	3	
	COMP	-0.3	3	
	PWRGD	-0.3	6	
	SS/TR	-0.3	3	
	RT/CLK	-0.3	6	
Output Voltage	BOOT-PH	0	7.5	V
	PH	-1	20	
	PH 10ns Transient	-3	20	
Vdiff (GND to exposed thermal pad)		-0.2	0.2	V
Source Current	RT/CLK		±100	μA
	PH		Current Limit	A
Sink Current	PH		Current Limit	A
	PVIN		Current Limit	
	COMP		±200	μA
	PWRGD	-0.1	5	mA
Electrostatic Discharge (HBM) QSS 009-105 (JESD22-A114A)			2	kV
Electrostatic Discharge (CDM) QSS 009-147 (JESD22-C101B.01)			500	V
Operating Junction Temperature		-40	125	°C
Storage Temperature		-65	150	

Table 12: Recommended operating conditions

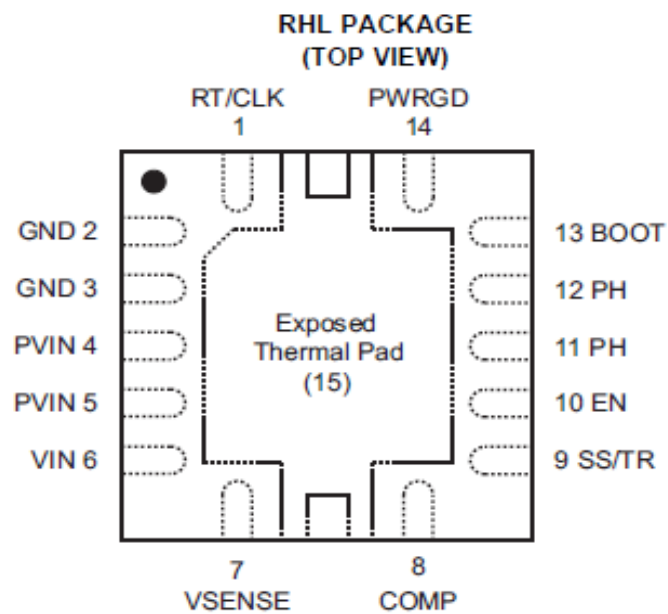


Figure 9: Pin Description

PIN		DESCRIPTION
NAME	NO.	
RT/CLK	1	Automatically selects between RT mode and CLK mode. An external timing resistor adjusts the switching frequency of the device; In CLK mode, the device synchronizes to an external clock.
GND	2, 3	Return for control circuitry and low-side power MOSFET.
PVIN	4, 5	Power input. Supplies the power switches of the power converter.
VIN	6	Supplies the control circuitry of the power converter.
VSENSE	7	Inverting input of the gm error amplifier.
COMP	8	Error amplifier output, and input to the output switch current comparator. Connect frequency compensation to this pin.
SS/TR	9	Slow-start and tracking. An external capacitor connected to this pin sets the internal voltage reference rise time. The voltage on this pin overrides the internal reference. It can be used for tracking and sequencing.
EN	10	Enable pin. Float to enable. Adjust the input undervoltage lockout with two resistors.
PH	11, 12	The switch node.
BOOT	13	A bootstrap cap is required between BOOT and PH. The voltage on this cap carries the gate drive voltage for the high-side MOSFET.
PWRGD	14	Power Good fault pin. Asserts low if output voltage is low due to thermal shutdown, dropout, over-voltage, EN shutdown or during slow start.
Exposed Thermal PAD	15	Thermal pad of the package and signal ground and it must be soldered down for proper operation.

Table 13: Pin functions.

D. TPS563200

General Description

TPS563200 are simple, easy-to-use, 3 A synchronous step-down (buck) converters in SOT-23 package. The devices are optimized to operate with minimum external component counts and also optimized to achieve low standby current. These switch mode power supply (SMPS) devices employ D-CAP2 mode control providing a fast transient response and supporting both low equivalent series resistance (ESR) output capacitors such as specialty polymer and ultra-low ESR ceramic capacitors with no external compensation components. TPS563200 operate in Advanced Eco-mode, which maintains high efficiency during light load operation. The devices are available in a 6-pin 1.6 x 2.9mm SOT (DDC) package, and specified from –40°C to 85°C of ambient temperature.

Features

- D-CAP2™ Mode Control with 650-kHz Switching Frequency
- Input Voltage Range: 4.5 V to 17 V
- Output Voltage Range: 0.76 V to 7 V
- Integrated 68-mΩ and 39-mΩ FETs
- Advanced Eco-mode™ Pulse-skip
- Low Shutdown Current Less than 10 μA
- 1% Feedback Voltage Accuracy (25°C)
- Startup from Pre-Biased Output Voltage
- Cycle-By-Cycle Hiccup Over-current Limit
- Non-latch OVP, UVLO and TSD Protections
- Fixed Soft Start: 1 ms

Applications

- Digital TV Power Supply
- High Definition Blu-ray Disc™ Players
- Networking Home Terminal
- Networking Home Terminal

			MIN	MAX	UNIT
V _{IN}	Supply input voltage range		4.5	17	V
V _I	Input voltage range	VBST	−0.1	23	V
		VBST (10 ns transient)	−0.1	26	
		VBST(vs SW)	−0.1	6	
		EN	−0.1	17	
		VFB	−0.1	5.5	
		SW	−1.8	17	
		SW (10 ns transient)	−3.5	20	
T _A	Operating free-air temperature		−40	85	°C

Table 14: Recommended operating conditions

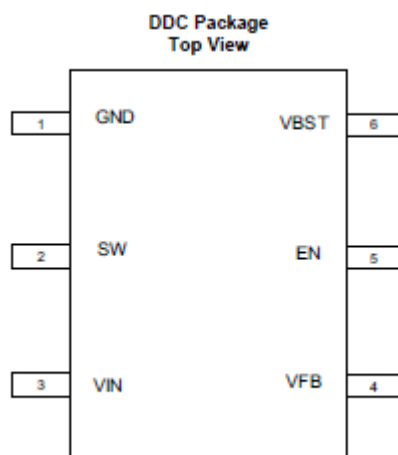


Figure 10: Pin Description

PIN		DESCRIPTION
NAME	NUMBER	
GND	1	Ground pin Source terminal of low-side power NFET as well as the ground terminal for controller circuit. Connect sensitive VFB to this GND at a single point.
SW	2	Switch node connection between high-side NFET and low-side NFET.
VIN	3	Input voltage supply pin. The drain terminal of high-side power NFET.
VFB	4	Converter feedback input. Connect to output voltage with feedback resistor divider.
EN	5	Enable input control. Active high and must be pulled up to enable the device.
VBST	6	Supply input for the high-side NFET gate drive circuit. Connect a 0.1μF capacitor between VBST and SW pins.

Table 15: Pin functions.

General Description

This P-Channel MOSFET is a rugged gate version of Fairchild Semiconductor's advanced PowerTrench process. It has been optimized for power management applications requiring a wide range of gate drive voltage ratings (4.5V – 20V).

Features

- –8.2 A, –40 V $R_{DS(ON)} = 0.027 \Omega @ V_{GS} = -10 \text{ V}$
 $R_{DS(ON)} = 0.035 \Omega @ V_{GS} = -4.5 \text{ V}$
- Fast switching speed
- High performance trench technology for extremely low $R_{DS(ON)}$
- High power and current handling capability

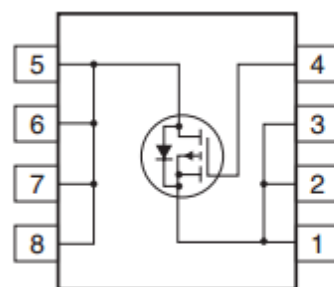
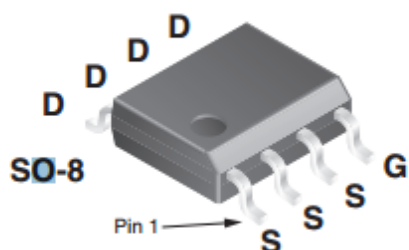


Figure 11: Pins

Absolute Maximum Ratings $T_A = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter		Ratings	Units
V _{DSS}	Drain-Source Voltage		−40	V
V _{GSS}	Gate-Source Voltage		±20	V
I _D	Drain Current	- Continuous (Note 1 a)	−8.2	A
		- Pulsed	−50	
P _D	Power Dissipation for Single Operation (Note 1 a)		2.5	W
	(Note 1 b)		1.4	
	(Note 1 c)		1.2	
T _J , T _{STG}	Operating and Storage Junction Temperature Range		−55 to +150	°C
Thermal Characteristics				
R _{θJA}	Thermal Resistance, Junction-to-Ambient	(Note 1 a)	50	°C/W
R _{θJA}	Thermal Resistance, Junction-to-Ambient	(Note 1 c)	125	
R _{θJC}	Thermal Resistance, Junction-to-Case	(Note 1)	25	

Table 16: Absolute maximum ratings

F.NTGS3446

Features

- Ultra Low $R_{DS(on)}$
- Higher Efficiency Extending Battery Life
- Logic Level Gate Drive
- Diode Exhibits High Speed, Soft Recovery
- Avalanche Energy Specified
- IDSS Specified at Elevated Temperature
- Pb-Free Package is Available

Applications

- Power Management in portable and battery-powered products, i.e. computers, printers, PCMCIA cards, cellular and cordless
- Lithium Ion Battery Applications
- Notebook PC

PIN ASSIGNMENT

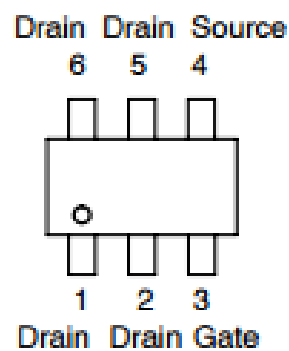


Figure 12: Pin description

MAXIMUM RATINGS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Rating	Symbol	Value	Unit
Drain-to-Source Voltage	V_{DSS}	20	V
Gate-to-Source Voltage	V_{GS}	± 12	V
Thermal Resistance Junction-to-Ambient (Note 1) Total Power Dissipation @ $T_A = 25^\circ\text{C}$ Drain Current - Continuous @ $T_A = 25^\circ\text{C}$ - Pulsed Drain Current ($t_p < 10 \mu\text{s}$)	$R_{\theta JA}$ P_d I_D I_{DM}	244 0.5 2.5 10	$^\circ\text{C/W}$ W A A
Thermal Resistance Junction-to-Ambient (Note 2) Total Power Dissipation @ $T_A = 25^\circ\text{C}$ Drain Current - Continuous @ $T_A = 25^\circ\text{C}$ - Pulsed Drain Current ($t_p < 10 \mu\text{s}$)	$R_{\theta JA}$ P_d I_D I_{DM}	128 1.0 3.6 14	$^\circ\text{C/W}$ W A A
Thermal Resistance Junction-to-Ambient (Note 3) Total Power Dissipation @ $T_A = 25^\circ\text{C}$ Drain Current - Continuous @ $T_A = 25^\circ\text{C}$ - Pulsed Drain Current ($t_p < 10 \mu\text{s}$)	$R_{\theta JA}$ P_d I_D I_{DM}	62.5 2.0 5.1 20	$^\circ\text{C/W}$ W A A
Source Current (Body Diode)	I_S	5.1	A
Operating and Storage Temperature Range	T_J, T_{stg}	-55 to 150	$^\circ\text{C}$
Maximum Lead Temperature for Soldering Purposes for 10 seconds	T_L	260	$^\circ\text{C}$

Table 17: Maximum ratings

G.APL5910**General Description**

The APL5910 is a 1A ultra low dropout linear regulator. The IC needs two supply voltages, one is a control voltage (VCNTL) for the control circuitry, the other is a main supply voltage (VIN) for power conversion, to reduce power dissipation and provide extremely low dropout voltage. The APL5910 integrates many functions. A Power-On- Reset (POR) circuit monitors both supply voltages on VCNTL and VIN pins to prevent erroneous operations. The functions of thermal shutdown and current-limit protect the device against thermal and current over-loads. A POK indicates that the output voltage status with a delay time set internally. It can control other converter for power sequence. The APL5910 can be enabled by other power systems. Pulling and holding the EN voltage below 0.4V shuts off the output.

The APL5910 is available in a SOP-8P package which features small size as SOP-8 and an Exposed Pad to reduce the junction-to-case resistance to extend power range of applications.

Features

- Ultra Low Dropout
 - 0.12V (Typical) at 1A Output Current
- 0.8V Reference Voltage
- High Output Accuracy
 - $\pm 1.5\%$ over Line, Load, and Temperature Range
- Fast Transient Response

- Adjustable Output Voltage
- Power-On-Reset Monitoring on Both VCNTL and VIN Pins
- Internal Soft-Start
- Current-Limit and ShortCurrent-Limit Protections
- Thermal Shutdown with Hysteresis
- Open-Drain VOUT Voltage Indicator (POK)
- Low Shutdown Quiescent Current (< 30mA)
- Shutdown/Enable Control Function
- Simple SOP-8P Package with Exposed Pad
- Lead Free and Green Devices Available (RoHS Compliant)

Applications

- Motherboards, VGA Cards
- Notebook PCs
- Add-in Cards

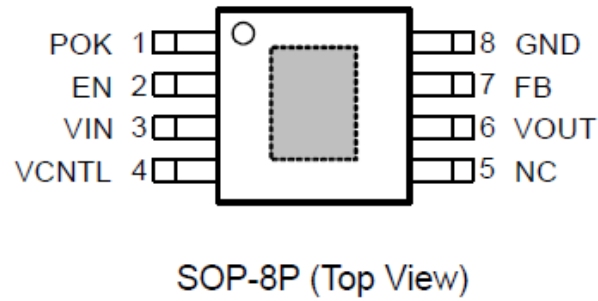


Figure 13: Pin configuration.

Symbol	Parameter		Range	Unit
V_{CNTL}	VCNTL Supply Voltage		3.0 ~ 5.5	V
V_{IN}	VIN Supply Voltage		1.0 ~ 5.5	V
V_{OUT}	VOUT Output Voltage (when $V_{CNTL}-V_{OUT}>1.4V$)		0.8 ~ $V_{IN} - V_{DROP}$	V
I_{OUT}	VOUT Output Current		0 ~ 1	A
R2	FB to GND		1k ~ 24k	Ω
C_{OUT}	VOUT Output Capacitance	$I_{OUT}=1A$ at 25% nominal V_{OUT}	8 ~ 600	μF
		$I_{OUT}=0.5A$ at 25% nominal V_{OUT}	8 ~ 900	
		$I_{OUT}=0.25A$ at 25% nominal V_{OUT}	8 ~ 1100	
ESR_{COUT}	ESR of VOUT Output Capacitor		0 ~ 200	m Ω
T_A	Ambient Temperature		-40 ~ 85	$^{\circ}C$
T_J	Junction Temperature		-40 ~ 125	$^{\circ}C$

Table 18: Recommended operating conditions.

PIN		FUNCTION
NO.	NAME	
1	POK	Power-OK signal output pin. This pin is an open-drain output used to indicate the status of output voltage by sensing FB voltage. This pin is pulled low when output voltage is not within the Power-OK voltage window.
2	EN	Active-high enable control pin. Applying and holding the voltage on this pin below the enable voltage threshold shuts down the output. When re-enabled, the IC undergoes a new soft-start process. When left this pin open, an internal pull-up current (5 μ A typical) pulls the EN voltage and enables the regulator.
3	VIN	Main supply input pin for voltage conversions. A decoupling capacitor ($\geq 10\mu$ F recommended) is usually connected near this pin to filter the voltage noise and improve transient response. The voltage on this pin is monitored for Power-On-Reset purpose
4	VCNTL	Bias voltage input pin for internal control circuitry. Connect this pin to a voltage source (+5V recommended). A decoupling capacitor (1 μ F typical) is usually connected near this pin to filter the voltage noise. The voltage at this pin is monitored for Power-On-Reset purpose.
5	NC	No Connection.
6	VOUT	Output pin of the regulator. Connecting this pin to load and output capacitors (10 μ F at least) is required for stability and improving transient response. The output voltage is programmed by the resistor-divider connected to FB pin. The VOUT can provide 1A (max.) load current to loads. During shutdown, the output voltage is quickly discharged by an internal pull-low MOSFET.
7	FB	Voltage Feedback Pin. Connecting this pin to an external resistor divider receives the feedback voltage of the regulator.

Table 19: Pin description.

H. APL2111H

General Description

The AP2111 is CMOS process low dropout linear regulator with enable function, the regulator delivers a guaranteed 600mA (Min) continuous load current. The AP2111 provides 1.2V, 1.5V, 1.8V, 2.5V, 3.3V, 4.8V regulated output and 0.8V to 5V adjustable output, and provides excellent output accuracy 1.5%, it is also provides a excellent load regulation, line regulation and excellent load transient performance due to very fast loop response. The AP2111 has built-in auto discharge function. The AP2111 features low power consumption. The AP2111 is available in SOIC-8, PSOP-8 SOT-223 and SOT-23-5 packages.

Features

- Output Voltage Accuracy: $\pm 1.5\%$
- Output Current: 600mA (Min)
- Foldback Short Current Protection: 50mA
- Enable Function to Turn On/Off VOUT
- Low Dropout Voltage (3.3V): 250mV (Typ) @ IOU=600Ma
- Excellent Load Regulation: 0.2%/A (Typ)
- Excellent Line Regulation: 0.02%/V (Typ)
- Low Quiescent Current: 55 μ A (Typ)
- Low Standby Current: 0.01 μ A (Typ)
- Low Output Noise: 50 μ VRMS
- PSRR: 65dB @ f=1kHz, 65dB @ f=100Hz
- OTSD Protection
- Stable with 1.0 μ F Flexible Cap: Ceramic, Tantalum and Aluminum Electrolytic
- Operating Temperature Range: -40°C to 85°C
- ESD: MM 400V, HBM 4000V

Applications

- LCD Monitor
- Portable DVD
- Laptop computer

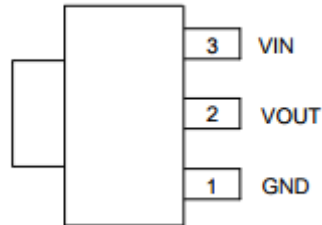


Figure 14: Pin configuration.

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{IN}	2.5		6.0	V
Operating Ambient Temperature Range	T_A	-40		85	°C

Table 20: Recommended operating conditions.

Pin Number				Pin Name	Function
SOIC-8/PSOP-8	SOT-223(H)	SOT-223(HA)	SOT-23-5		
4	3	2	3	VIN	Input voltage
2	2	3	4	VOUT	Output voltage
8			1	EN	Chip enable, H – normal work, L – shutdown output
1, 3, 5, 6, 7	1	1	2	GND	Ground
			5	ADJ/NC	Adjust output for ADJ version/No connected for fixed version

Table 21: Pin description.

6. 2GB DDR3 SDRAM

HYNIX H5TQ2G63GFR

Description

The H5TQ2G83GFR-xxC, H5TQ2G63GFR-xxC, H5TQ2G83GFR-xxI, H5TQ2G63GFR-xxI, H5TQ2G83GFR-xxL, H5TQ2G63GFR-xxL, H5TQ2G83GFR-xxJ, H5TQ2G63GFR-xxJ are a 2, 147, 483, 648-bit CMOS Double Data Rate III (DDR3) Synchronous DRAM, ideally suited for the main memory applications which requires large memory density and high bandwidth. SK Hynix 2Gb DDR3 SDRAMs offer fully synchronous operations referenced to both rising and falling edges of the clock. While all addresses and control inputs are latched on the rising edges of the CK (falling edges of the CK), Data, Data strobes and Write data masks inputs are sampled on both rising and falling edges of it. The data paths are internally pipelined and 8-bit prefetched to achieve very high bandwidth.

Features

- VDD=VDDQ=1.5V +/- 0.075V
- Fully differential clock inputs (CK, $\overline{\text{CK}}$) operation
- Differential Data Strobe (DQS, $\overline{\text{DQS}}$)
- On chip DLL align DQ, DQS and $\overline{\text{DQS}}$ transition with CK transition
- DM masks write data-in at the both rising and falling edges of the data strobe
- All addresses and control inputs except data, data strobes and data masks latched on the rising edges of the clock
- Programmable CAS latency 5, 6, 7, 8, 9, 10, 11, 12, 13 and 14 supported
- Programmable additive latency 0, CL-1, and CL-2 supported
- Programmable CAS Write latency (CWL) = 5, 6, 7, 8 9 and 10
- Programmable burst length 4/8 with both nibble sequential and interleave mode
- BL switch on the fly
- 8banks
- Average Refresh Cycle (Tcase 0 °C~95 °C)
 - 7.8 μs at 0°C ~ 85 °C
 - 3.9 μs at 85°C ~ 95 °C
- Commercial Temperature(0°C ~ 95 °C)
- Industrial Temperature(-40°C ~ 95 °C)
- JEDEC standard 78ball FBGA(x8), 96ball FBGA(x16)
- Driver strength selected by EMRS
- Dynamic On Die Termination supported
- Asynchronous RESET pin supported
- ZQ calibration supported
- TDQS (Termination Data Strobe) supported (x8 only)
- Write Levelization supported
- 8 bit pre-fetch

Symbol	Parameter	Rating			Units	Notes
		Min.	Typ.	Max.		
VDD	Supply Voltage	1.425	1.500	1.575	V	1,2
VDDQ	Supply Voltage for Output	1.425	1.500	1.575	V	1,2

Notes:

1. Under all conditions, VDDQ must be less than or equal to VDD.
2. VDDQ tracks with VDD. AC parameters are measured with VDD and VDDQ tied together.

Table 22: Recommended operating conditions.

7. 4GB DDR3L SDRAM

HYNIX H5TQ4G63GFR

Description

The H5TC4G83CFR-xxA(I,L,J),H5TQC4G63CFR-xxA(I,L,J) are a 4Gb low power Double Data Rate III (DDR3L) Synchronous DRAM, ideally suited for the main memory applications which requires large memory density, high bandwidth and low power operation at 1.35V. SK Hynix DDR3L SDRAM provides backward compatibility with the 1.5V DDR3 based environment without any changes. SK Hynix 4Gb DDR3L SDRAMs offer fully synchronous operations referenced to both rising and falling edges of the clock. While all addresses and control inputs are latched on the rising edges of the clock (falling edges of the clock), data, data strobes and write data masks inputs are sampled on both rising and falling edges of it. The datapaths are internally pipelined and 8-bit prefetched to achieve very high bandwidth.

Features

- VDD=VDDQ=1.35V + 0.100 / - 0.067V
- Fully differential clock inputs (CK, $\overline{\text{CK}}$) operation
- Differential Data Strobe (DQS, $\overline{\text{DQS}}$)
- On chip DLL align DQ, DQS and $\overline{\text{DQS}}$ transition with CK transition
- DM masks write data-in at the both rising and falling edges of the data strobe
- All addresses and control inputs except data, data strobes and data masks latched on the rising edges of the clock
- Programmable CAS latency 5, 6, 7, 8, 9, 10, 11 and 13 supported
- Programmable additive latency 0, CL-1, and CL-2 supported
- Programmable CAS Write latency (CWL) = 5, 6, 7, 8
- Programmable burst length 4/8 with both nibble sequential and interleave mode
- BL switch on the fly
- 8banks
- Average Refresh Cycle (Tcase of 0 °C~95 °C)
 - 7.8 μs at 0 °C ~ 85 °C
 - 3.9 μs at 85 °C ~ 95 °C
- Commercial Temperature(0 °C ~ 95 °C)
- Industrial Temperature(-40 °C ~ 95 °C)
- JEDEC standard 78ball FBGA(x8), 96ball FBGA (x16)
- Driver strength selected by EMRS
- Dynamic On Die Termination supported
- Asynchronous RESET pin supported
- ZQ calibration supported
- TDQS (Termination Data Strobe) supported (x8 only)
- Write Levelization supported
- 8 bit pre-fetch

Symbol	Parameter	Rating	Units	Notes
VDD	Voltage on VDD pin relative to Vss	- 0.4 V ~ 1.80 V	V	1,3
VDDQ	Voltage on VDDQ pin relative to Vss	- 0.4 V ~ 1.80 V	V	1,3
V _{IN} , V _{OUT}	Voltage on any pin relative to Vss	- 0.4 V ~ 1.80 V	V	1
T _{STG}	Storage Temperature	-55 to +100	°C	1, 2

Notes:

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Storage Temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JEDEC51-2 standard.
3. VDD and VDDQ must be within 300mV of each other at all times; and VREF must not be greater than 0.6XVDDQ. When VDD and VDDQ are less than 500mV; VREF may be equal to or less than 300mV.

Table 23: Absolute Maximum DC Ratings

Recommended DC Operating Conditions - DDR3L (1.35V) operation

Symbol	Parameter	Rating			Units	Notes
		Min.	Typ.	Max.		
VDD	Supply Voltage	1.283	1.35	1.45	V	1,2,3,4
VDDQ	Supply Voltage for Output	1.283	1.35	1.45	V	1,2,3,4

Notes:

1. Maximum DC value may not be greater than 1.425V. The DC value is the linear average of VDD/VDDQ (t) over a very long period of time (e.g., 1 sec).
2. If maximum limit is exceeded, input levels shall be governed by DDR3 specifications.
3. Under these supply voltages, the device operates to this DDR3L specification.
4. Once initialized for DDR3L operation, DDR3 operation may only be used if the device is in reset while VDD and VDDQ are changed for DDR3 operation (see Figure 0).

Recommended DC Operating Conditions - DDR3L (1.5V) operation

Symbol	Parameter	Rating			Units	Notes
		Min.	Typ.	Max.		
VDD	Supply Voltage	1.425	1.5	1.575	V	1,2,3
VDDQ	Supply Voltage for Output	1.425	1.5	1.575	V	1,2,3

Notes:

1. If minimum limit is exceeded, input levels shall be governed by DDR3L specifications.
2. Under 1.5V operation, this DDR3L device operates to the DDR3 specifications under the same speed timings as defined for this device.
3. Once initialized for DDR3 operation, DDR3L operation may only be used if the device is in reset while VDD and VDDQ are changed for DDR3L operation (see Figure 0).

Table 24: Recommended operating conditions.

8. 32GBIT (4G X 8 BIT) NAND FLASH MEMORY

MT29F4G08ABAEAWP

Key Features

- Open NAND Flash Interface (ONFI) 1.0-compliant¹
- Single-level cell (SLC) technology
- Organization
 - Page size x8: 4320 bytes (4096 + 224 bytes)
 - Page size x16: 2160 words (2048 + 112 words)
 - Block size: 64 pages (256K + 14K bytes)
 - Plane size: 2 planes x 1024 blocks per plane
 - Device size: 4Gb: 2048 blocks
- Asynchronous I/O performance
 - ^tRC/^tWC: 20ns (3.3V), 30ns (1.8V)
- Array performance
 - Read page: 25μs
 - Program page: 200μs (TYP)
 - Erase block: 2ms (TYP)
- Command set: ONFI NAND Flash Protocol
- Advanced command set
 - Program page cache mode
 - Read page cache mode
 - One-time programmable (OTP) mode
 - Block lock (1.8V only)
 - Programmable drive strength
 - Two-plane commands
 - Multi-die (LUN) operations
 - Read unique ID
 - Internal data move
- Operation status byte provides software method for detecting
 - Operation completion
 - Pass/fail condition
 - Write-protect status
- Ready/Busy# (R/B#) signal provides a hardware method of detecting operation completion
- WP# signal: Write protect entire device
- First block (block address 00h) is valid when shipped from factory with ECC. For minimum required ECC, see Error Management.
- RESET (FFh) required as first command after power-on
- Alternate method of device initialization after power up (contact factory)
- Internal data move operations supported within the plane from which data is read
- Quality and reliability
 - Data retention: JESD47G-compliant; see qualification report
 - Endurance: 60,000 PROGRAM/ERASE cycles
- Operating voltage range
 - V_{CC}: 2.7–3.6V
 - V_{CC}: 1.7–1.95V
- Operating temperature:
 - Commercial: 0°C to +70°C
 - Industrial (IT): –40°C to +85°C
- Package
 - 48-pin TSOP type 1, CPL²
 - 63-ball VFBGA

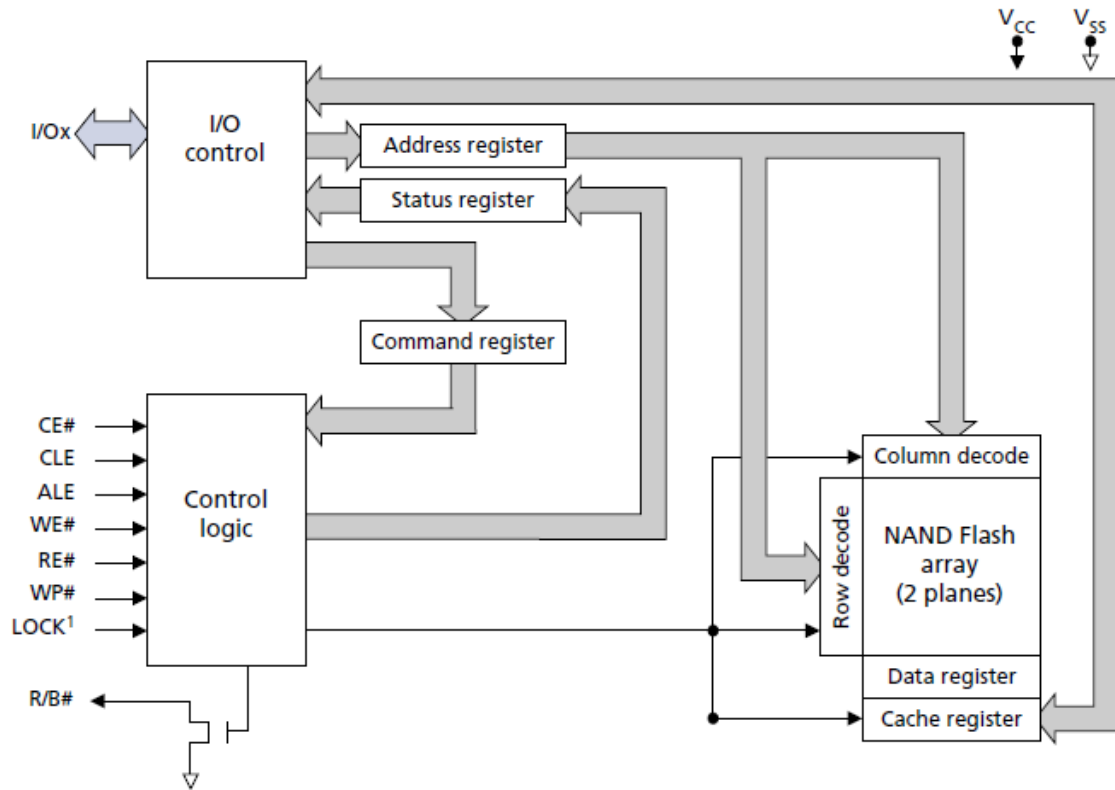
Notes: 1. The ONFI 1.0 specification is available at www.onfi.org.
2. CPL = Center parting line.

Description

Micron NAND Flash devices include an asynchronous data interface for high-performance I/O operations. These devices use a highly multiplexed 8-bit bus (I/Ox) to transfer commands, address, and data. There are five control signals used to implement the asynchronous data interface: CE#, CLE, ALE, WE#, and RE#. Additional signals control hardware write protection and monitor device status (R/B#).

This hardware interface creates a low pin-count device with a standard pinout that remains the same from one density to another, enabling future upgrades to higher densities with no board redesign. A target is the unit of memory accessed by a chip enable signal.

A target contains one or more NAND Flash die. A NAND Flash die is the minimum unit that can independently execute commands and report status. A NAND Flash die, in the ONFI specification, is referred to as a logical unit (LUN). There is at least one NAND Flash die per chip enable signal. For further details, see Device and Array Organization.



Note: 1. The LOCK pin is used on the 1.8V device.

Figure 15:Functional block diagram

Parameter	Conditions	Symbol	Min	Typ	Max	Unit	Notes
Sequential READ current	$t_{RC} = t_{RC} (MIN)$; $CE\# = V_{IL}$; $I_{OUT} = 0mA$	I_{CC1}	–	15	30	mA	4
PROGRAM current	–	I_{CC2}	–	15	30	mA	4
ERASE current	–	I_{CC3}	–	15	30	mA	4
Standby current (TTL)	$CE\# = V_{IH}$; $WP\# = 0V/V_{CC}$	I_{SB1}	–	–	1	mA	
Standby current (CMOS)	$CE\# = V_{CC} - 0.2V$; $WP\# = 0V/V_{CC}$	I_{SB2}	–	20	100	μA	
Staggered power-up current	Rise time = 1ms Line capacitance = 0.1 μF	I_{ST}	–	–	10 per die	mA	1
Input leakage current	$V_{IN} = 0V$ to V_{CC}	I_{LI}	–	–	± 10	μA	
Output leakage current	$V_{OUT} = 0V$ to V_{CC}	I_{LO}	–	–	± 10	μA	
Input high voltage	I/O[7:0], I/O[15:0], $CE\#, CLE, ALE, WE\#, RE\#, WP\#, R/B\#$	V_{IH}	$0.8 \times V_{CC}$	–	$V_{CC} + 0.3$	V	
Input low voltage, all inputs	–	V_{IL}	–0.3	–	$0.2 \times V_{CC}$	V	
Output high voltage	$I_{OH} = -400\mu A$	V_{OH}	$0.67 \times V_{CC}$	–	–	V	2
Output low voltage	$I_{OL} = -2.1mA$	V_{OL}	–	–	0.4	V	2
Output low current	$V_{OL} = 0.4V$	$I_{OL} (R/B\#)$	8	10	–	mA	3

- Notes: 1. Measurement is taken with 1ms averaging intervals and begins after V_{CC} reaches $V_{CC} (MIN)$.
2. $I_{OL} (R/B\#)$ may need to be relaxed if R/B pull-down strength is not set to full.
3. V_{OH} and V_{OL} may need to be relaxed if I/O drive strength is not set to full.

Table 25: DC Characteristics and Operating Conditions (3.3V)

9. 16M-BIT [16M X 1] CMOS SERIAL FLASH EEPROM

A. *MX25L1606E SPI FLASH*

Features

General

- Single Power Supply Operation
 - 2.7 to 3.6 volt for read, erase, and program operations
- Serial Peripheral Interface compatible -- Mode 0 and Mode 3
- 8M: 8,388,608 x 1 bit structure or 4,194,304 x 2 bits (Dual Output mode) structure
16M: 16,777,216 x 1 bit structure or 8,388,608 x 2 bits (Dual Output mode) structure
- 256 Equal Sectors with 4K byte each (8Mb)
512 Equal Sectors with 4K byte each (16Mb)
 - Any Sector can be erased individually
- 16 Equal Blocks with 64K byte each (8Mb)
32 Equal Blocks with 64K byte each (16Mb)
 - Any Block can be erased individually
- Program Capability
 - Byte base
 - Page base (256 bytes)
- Latch-up protected to 100mA from -1V to Vcc +1V

Performance

- High Performance
 - Fast access time: 86MHz serial clock
 - Serial clock of Dual Output mode : 80MHz
 - Fast program time: 1.4ms(typ.) and 5ms(max.)/page
 - Byte program time: 9us (typical)
 - Fast erase time: 60ms(typ.) /sector ; 0.7s(typ.) /block
- Low Power Consumption
 - Low active read current: 16Mb: 25mA(max.) at 86MHz; 8Mb: 12mA(max.) at 86MHz
 - Low active programming current: 20mA (max.)
 - Low active erase current: 20mA (max.)
 - Low standby current: 25uA (max.)
 - Deep power-down mode 5uA (typical)
- Typical 100,000 erase/program cycles
- 20 years of data retention

Software Features

- Input Data Format
 - 1-byte Command code
- Advanced Security Features
 - Block lock protection
 - The BP3-BP0(16Mb) ; BP2-BP0(8Mb) status bit defines the size of the area to be software protection against program and erase instructions
 - Additional 512 bit secured OTP for unique identifier
- Auto Erase and Auto Program Algorithm
 - Automatically erases and verifies data at selected sector

- Automatically programs and verifies data at selected page by an internal algorithm that automatically times the program pulse widths (Any page to be programmed should have page in the erased state first)6
P/N: PM1548 REV. 1.2, JUL. 02, 2010 MX25L8006E MX25L1606E
- Status Register Feature
- Electronic Identification
 - JEDEC 1-byte manufacturer ID and 2-byte device ID
 - RES command for 1-byte Device ID
 - REMS commands for 1-byte manufacturer ID and 1-byte device ID

Hardware Features

- PACKAGE
 - 16-pin SOP (300mil), MX25L1606E only
 - 8-pin SOP (150mil)
 - 8-pin SOP (200mil)
 - 8-pin PDIP (300mil)
 - 8-land WSON (6x5mm)
 - 8-land USON (4x4mm)
 - All Pb-free devices are RoHS Compliant

General Description

The device feature a serial peripheral interface and software protocol allowing operation on a simple 3-wire bus. The three bus signals are a clock input (SCLK), a serial data input (SI), and a serial data output (SO). Serial access to the device is enabled by CS# input.

When it is in Dual Output read mode, the SI and SO pins become SIO0 and SIO1 pins for data output.

The device provides sequential read operation on whole chip.

After program/erase command is issued, auto program/ erase algorithms which program/ erase and verify the specified page or sector/block locations will be executed. Program command is executed on byte basis, or page basis, or word basis for erase command is executes on sector, or block, or whole chip basis.

To provide user with ease of interface, a status register is included to indicate the status of the chip. The status read command can be issued to detect completion status of a program or erase operation via WIP bit.

Advanced security features enhance the protection and security functions, please see security features section for more details.

When the device is not in operation and CS# is high, it is put in standby mode.

The device utilizes Macronix's proprietary memory cell, which reliably stores memory contents even after typical 100,000 program and erase cycles.

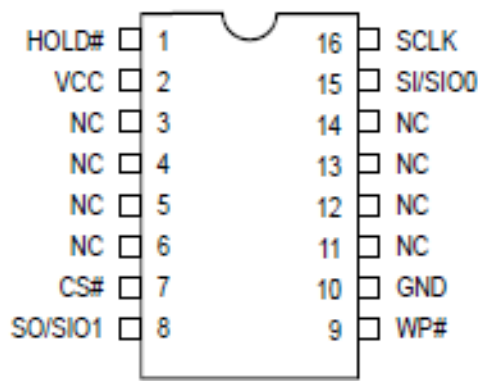


Figure 16: Pin configuration.

SYMBOL	DESCRIPTION
CS#	Chip Select
SI/SIO0	Serial Data Input (for 1 x I/O)/ Serial Data Input & Output (for Dual Output mode)
SO/SIO1	Serial Data Output (for 1 x I/O)/ Serial Data Output (for Dual Output mode)
SCLK	Clock Input
WP#	Write protection
HOLD#	Hold, to pause the device without deselecting the device
VCC	+ 3.3V Power Supply
GND	Ground

Table 26: Pin description.

B. M25Q32FV SPI FLASH

Key Features

- **New Family of SpiFlash Memories**
 - W25Q32FV: 32M-bit/ 4M-byte
 - Standard SPI: CLK, /CS, DI, DO, /WP, /Hold
 - Dual SPI: CLK, /CS, IO₀, IO₁, /WP, /Hold
 - Quad SPI: CLK, /CS, IO₀, IO₁, IO₂, IO₃
 - QPI: CLK, /CS, IO₀, IO₁, IO₂, IO₃
 - Software & Hardware Reset
- **Highest Performance Serial Flash**
 - 104MHz Single, Dual/Quad SPI clocks
 - 208/416Mhz equivalent Dual/Quad SPI
 - 50 MB/S continuous data transfer rate
 - More than 100,000 erase/program cycles
 - More than 20-year retention
- **Efficient “Continuous Read” and QPI Mode**
 - Continuous Read with 8/16/32/64-Byte Wrap
 - As few as 8 clocks to address memory
 - Quad Peripheral Interface (QPI) reduces instruction overhead
 - Allows true XIP (execute in place) operation

- Outperforms X16 Parallel Flash
- **Low Power, Wide Temperature Range**
 - Single 2.7 to 3.6V supply
 - 4mA active current, <1uA Power-down(typ.)
 - -40C to +85C operating range
- **Flexible Architecture with 4KB sectors**
 - Uniform Sector/Block Erase (4K/32K/64K-Byte)
 - Program 1 to 256 byte per programmable page
 - Erase/Program Suspend&Resume
- **Advanced Security Features**
 - Software and Hardware Write-Protect
 - Power Supply Lock-Down and OTP protection
 - Top/Bottom, Complement array protection
 - Individual Block/Sector array protection
 - 64-Bit Unique ID for each device
 - Discoverable Parameters (SFDP) Register
 - 3x256-Bytes Security Registers with OTP locks
 - Volatile & Non-volatile Status Register Bits
- **Space Efficient Packaging**
 - 8-pin SOIC 208-mil / VSOP 208-mil
 - 8-pad WSON 6x5-mm / 8x6-mm
 - 16-pin SOIC 300-mil (additional / RESET pin)
 - 8-pin PDIP 300-mil
 - 24-ball TFBGA 8x6-mm (6x4/5x5 ball array)
 - Contact Winbond for KGB and other options

General Description

This W25Q32FV (32M-bit) Serial Flash memory provides a storage solution for systems with limited space, pins and power. The 25Q series offers flexibility and performance well beyond ordinary Serial Flash devices. They are ideal for code shadowing to RAM, executing code directly from Dual/Quad SPI (XIP) and storing voice, text and data. The device operates on a single 2.7V to 3.6V power supply with current consumption as low as 4mA active and 1uA for power-down. All devices are offered in space-saving packages.

The W25Q32FV array is organized into 16,384 programmable pages of 256-bytes each. Up to 256 bytes can be programmed at a time. Pages can be erased in groups of 16 (4KB sector erase), groups of 128 (32KB block erase), groups of 256 (64KB block erase) or the entire chip (chip erase). The W25Q32FV has 1,024 erasable sectors and 64 erasable blocks respectively. The small 4KB sectors allow for greater flexibility in applications that require data and parameter storage.

The W25Q32FV support the standart Serial Peripheral Interface (SPI), Dual/Quad I/O SPI as well as 2-clocks instruction cycle Quad Periphareel Interface (QPI): Serial Clock, Chip Select, Serial Data I/O0 (DI), I/O1 (D0), I/O2 (/WP), and I/O3 (/HOLD). SPI clock frequencies of up to 104MHz are supported allowing equivalent clock rates of 208MHz (104MHz x 2) for Duad I/O and 416Mhz (104MHz x 4) for Quad I/O when using the Fast Read Dual/Quad I/O and QPI instructions. These transfer rates can outperform standart Asynchronous 8 an 16-bit Parallel Flash memories. The Continuous Read Mode allows for efficient memory Access with as few as 8-clocks of instruction-overhead to read a 24-bit address, allowing true XIP(execute in place) operation.

A Hold pin, Write Protect pin and programmable write protection, with top or bottom array control, provide further control flexibility. Additionally, the device supports JEDEC standart manufacturer and device ID and SFDP Register, a 64-bit Unique Serial Number and three 256-bytes Security Registers.

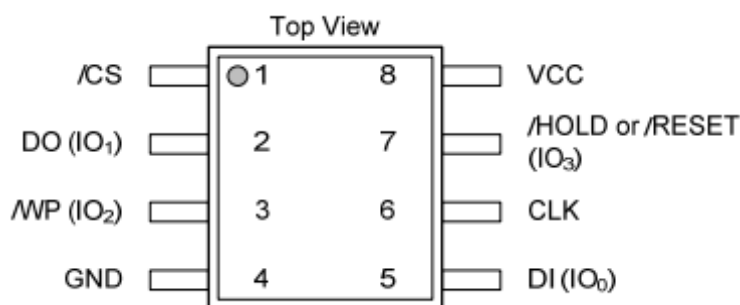


Figure 17: Pin configuration.

PIN NO.	PIN NAME	I/O	FUNCTION
1	/CS	I	Chip Select Input
2	DO (IO1)	I/O	Data Output (Data Input Output 1) ⁽¹⁾
3	/WP (IO2)	I/O	Write Protect Input (Data Input Output 2) ⁽²⁾
4	GND		Ground
5	DI (IO0)	I/O	Data Input (Data Input Output 0) ⁽¹⁾
6	CLK	I	Serial Clock Input
7	/HOLD or /RESET (IO3)	I/O	Hold or Reset Input (Data Input Output 3) ⁽²⁾
8	VCC		Power Supply

Notes:

1. IO0 and IO1 are used for Standard and Dual SPI instructions
2. IO0 – IO3 are used for Quad SPI instructions, /WP & /HOLD (or /RESET) functions are only available for Standard/Dual SPI.

Table 27: Pin description.

10. STDP4320 (DP1.2 SPLITTER IC)

General Description

The STDP4320 is a high-speed DisplayPort dual mode splitter IC targeted for audio-video demultiplexing and routing in applications such as notebooks, docking stations, video hub, 4K2K TVs, daisy chainable monitors, digital signage, etc. It consists of one dual mode input port and two dual mode output ports configurable as either DisplayPort or HDMI/DVI. STDP4320 is a VESA DP Standard Ver. 1.2a compliant device that supports advanced features such as MST, HBR2, 3D formats and GTC assist. Designs based on STDP4320 have the flexibility to offer either DP or HDMI/DVI connectors on its end product to interface with legacy and new generation video sources and sinks. In addition, STDP4320-based products with a DisplayPort output connector are DP++ compliant and work with any HDMI or single link DVI sink through a passive level translator (dongle). The STDP4320 uses MegaChips' latest generation DisplayPort dual mode receiver and transmitter technology that supports both DisplayPort and TMDS signal formats. This device receives MST format up to eight audio-video streams, which can be further routed on either of the two outputs in any combination of eight streams depending on the capability of downstream sinks. This device can also replicate the incoming video streams on both output ports simultaneously, thus allowing cloning on two downstream sinks. For example, a 4K2K 60 Hz video input is replicated on two output ports simultaneously. The DisplayPort receiver and transmitters support HBR2 speed, a data rate of 5.4 Gbps per lane with a total bandwidth of 21.6 Gbps link rate. In HDMI mode, this device supports link rates up to 3.2 Gbps corresponding to a pixel rate of 300 MHz, adequate for supporting video resolution up to FHD 120 Hz with all 3D formats. The device is also capable of delivering deep color video up to 16-bits per color. The STDP4320 allows audio transport from the source to the desired audio rendering devices over the video output port or through an SPDIF

port. The STDP4320 supports RGB and YCbCr colorimetric formats with color depth of 16, 12, 10, and 8 bits. The STDP4320 features the HDCP 1.3 content protection scheme with embedded keys for secure transmission of protected audio-video content. It also operates as an HDCP repeater for the downstream sinks. The DDC ports in the STDP4320 allow the upstream source to access EDID and transfer MCCS commands to downstream sinks when the physical ports are either HDMI or DVI type. If both the upstream source and downstream sinks are DP type, I2C transactions take place over the AUX CH. If one of them is a DP type and the other is either a HDMI or DVI type, STDP4320 converts the I2C over AUX message protocol to I2C commands and sends it on the DDC port.

Features

- DisplayPort dual mode receiver;
 - DP 1.2a compliant
 - Link rate HBR2/HBR/RBR
 - SST or MST (up to eight streams)
 - 1, 2, or 4 lanes
 - AUX CH 1 Mbps
 - HPD out
 - HDMI/DVI operation (3.2 Gbps link rate)
 - Functions as eDP and MyDP receiver
- DisplayPort dual mode transmitters
 - Two transmitter ports
 - DP 1.2a compliant
 - Link rate HBR2/HBR/RBR
 - SST or MST (up to eight streams)
 - 1, 2, or 4 lanes
 - AUX CH 1 Mbps
 - HPD in
 - HDMI/DVI operation (3.2 Gbps link rate) with external level translator
 - Functions as eDP transmitter
- SPDIF audio output
 - Two SPDIF port pins
 - 192 kHz/24 bits
 - Compressed/LPCM
- Conversion from DP SST to TMDS format and vice versa
- HDCP repeater with embedded keys
- AUX to I2C bridge for EDID/MCCS pass through
 - Maps on DDC ports
- Device configuration options
 - SPI Flash
 - I2C host interface
- Deep color support
 - RGB/YCC (4:4:4) – 16-bit color
 - YCC (4:2:2) – 16-bit color
- Spread spectrum on DisplayPort interface for EMI reduction
- Bandwidth
 - Video resolution up to 4K2K @ 60 Hz
 - Audio 7.1 Ch up to 192 kHz sample rate
- Low power operation
 - Standby 30 mW
- Package
 - 172 LFBGA (12 x 12 mm)
- Power supply voltages
 - 3.3 V I/O; 1.2 V core

Applications

Audio-video router for PC/notebooks, docking stations, hub, 4K2K TVs, daisy chain monitors, digital signage

11. EP9162S & EPF025R (HDMI 2.0A / HDCP2.2 SPLITTER IC)

A. EP9162S

General Description

EP9162S is a 2-Port DVI/HDMI 1.4b/HDMI 2.0a splitter with integrated HDCP 1.4 and HDCP 2.2 decryption/encryption engines. EP9162S receives DVI/HDMI 1.4b/HDMI 2.0a inputs, process HDCP 1.4 or HDCP 2.2 decryption and encryption again, then transmits the data to 2 DVI/HDMI 1.4b/HDMI 2.0a ports. The chip also supports HDCP 1.4 to HDCP 2.2 and HDCP 2.2 to HDCP 1.4 conversions.

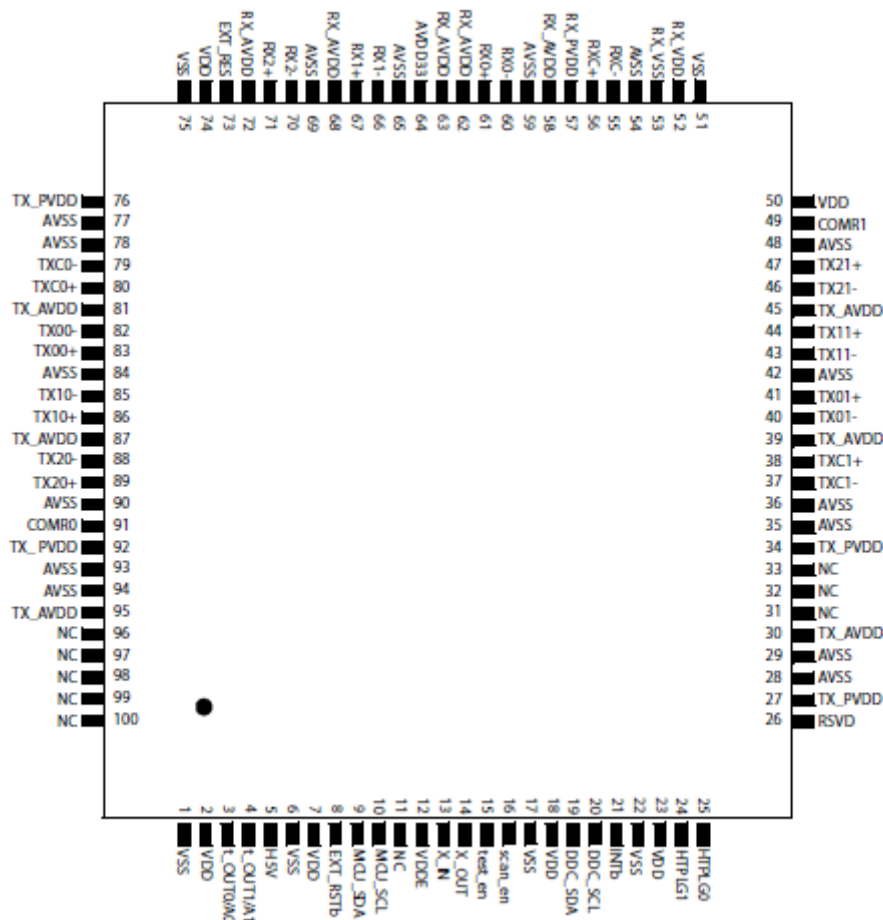


Figure 18: Pin Configuration

Features

- On-chip HDMI Receiver and Transmitter core which are compliant with DVI 1.0, HDMI 1.4b and HDMI 2.0a specification
- On-chip HDCP RX/TX ciphers which are compliant with HDCP 1.4/2.2 specification
- Wide Frequency Range: 25MHz - 600MHz
- Support Jitter Clean capability for more cascable stages
- Supports 12-bit Deep Full HD, Full 3D, HDR and 4K2K 60Hz video
- Supports 1 DVI/HDMI input port and 2 DVI/HDMI output ports
- Supports conversion of HDMI signalling to DVI/HDMI signalling
- Support HDCP 1.4 to HDCP 2.2 conversion
- Support HDCP 2.2 to HDCP 1.4 conversion
- Support on-chip 512 byte E-DDC EDID RAM for input port.

- Cascadable to make more than 2 output ports
- Provide companion HDCP 2.2 Controller (EPF025R) with integrated HDCP keys.
- 100-pin TQFP EPAD package

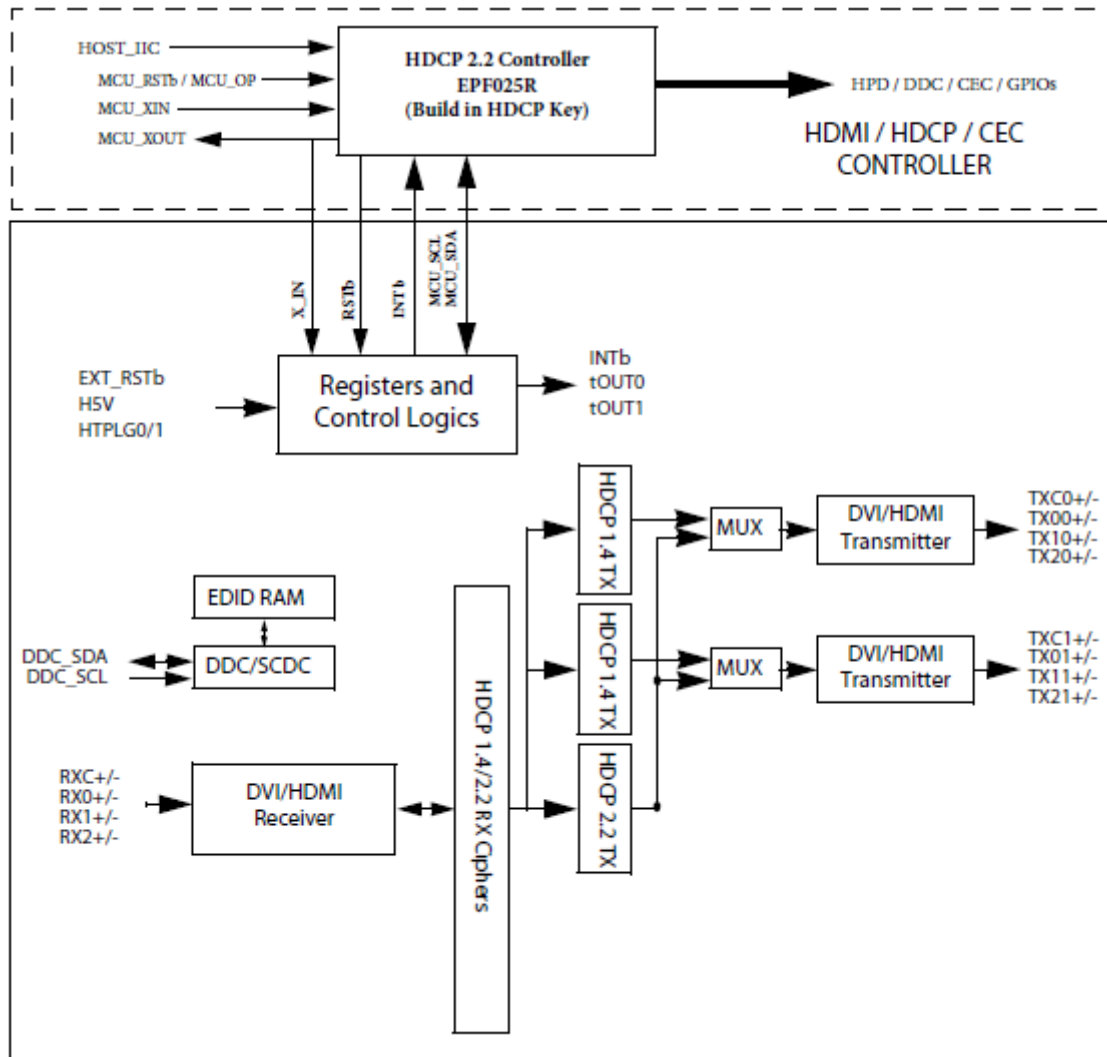


Figure 19: Block Diagram

B. EP025R

General Description

EPF025R is a HDCP 2.2 Controller for Explore HDMI 2.0 chips which has HDCP 2.2 function. It can handle the HDCP 2.2 authentication and ALU calculation for both HDCP 2.2 RX or TX. The EPF025R also provide the miscellaneous controls of HDMI 2.0 function. It can support the Software DDC up to 4 port, Hot-Plug signal detect/control, and CEC. The EPF025R has embedded Flash that provide the HDCP Key storage. It can also provide the EDID storage.

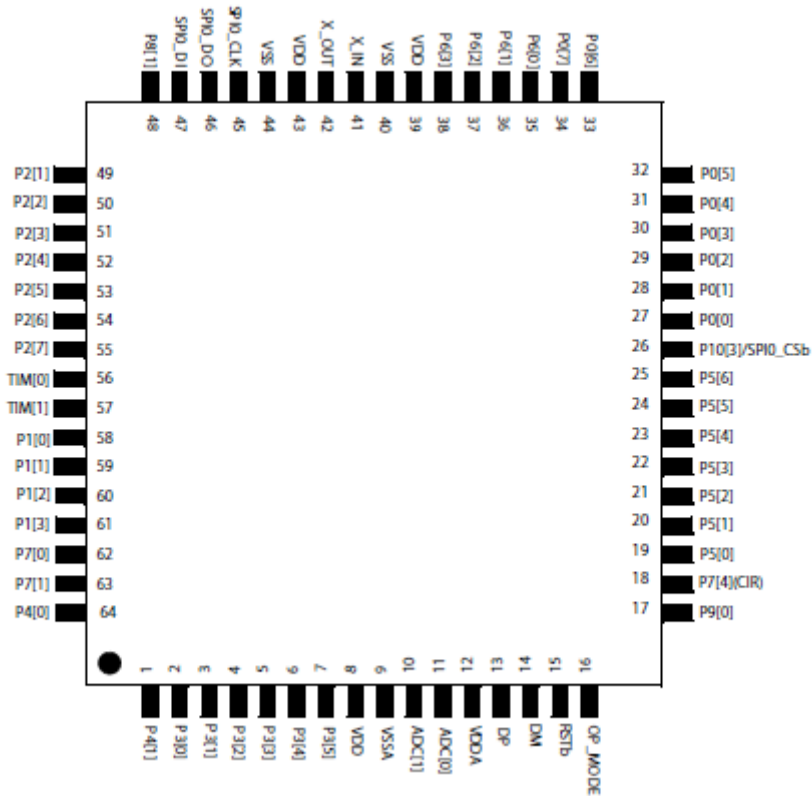


Figure 20: Pin Configuration

Features

- On-chip 80515 core with 128K bytes Flash, 256 bytes Direct RAM and 4K bytes on-chip auxiliary RAM
- Fast CPU rate (24Mhz). 41.6 ns for shortest instruction
- Programmable CPU clocks from 24 Mhz to 500 Khz
- Programmable crystal start-up cycles from 0 to 4096 cycles
- Supports Idle mode and Stop mode for power saving.
- Supports crystal/CPU wake-up from Stop mode
- Supports In Circuit Flash programming (ICP)
- Supports 2 external interrupts
- Supports keyboard interrupt on 4 GPIO pins.
- Support HDCP 1.4/2.2 Authentication control
- Support Embedded HDCP 1.4/2.2 Key
- On-chip high speed IIC Master and IIC Slave ports with configurable pin outs (SMBUS0 Master can support up to 1.5MHz clock rate)
- On-chip USB 1.1 host/slave which supports end-pint 0, 1, 2 and 64-byte bulk transfer
- On-chip 4 Timers supporting Timer, Pulse Output, Event Counter and Pulse Width Measurement modes
- Support primary and secondary crystal clock selection for Timer
- On-chip 15-bit programmable Watchdog Timer
- On-chip Serial Port which supports Synchronous mode and 8/9-bit UART modes
- On-chip 1 port of Serial Peripheral Interface (SPI) supporting both Master and Slave modes
- On-chip 1 channel of 8-bit PWM with programmable repetition rate
- On-chip 2 channels of 10-bit ADC
- On-chip Consumer Infra-Red Remote Receiver (CIR) which supports NEC and Phillips RC-5/RC-6 protocols
- Supports 45 General Purpose I/O Pins and most of the I/O pins are 5V tolerant.
- Timer, SPI, ADC and USB pins can be additional GPIO if the associated function is not enabled

- On-chip Low Voltage Inhibit (LVI) circuit which provides reliable power up reset and prevent accidental data loss in Flash
- Single 3.3V CMOS design
- 64-pin LQFP package (body size 7mm x 7mm) (Pb-Free)

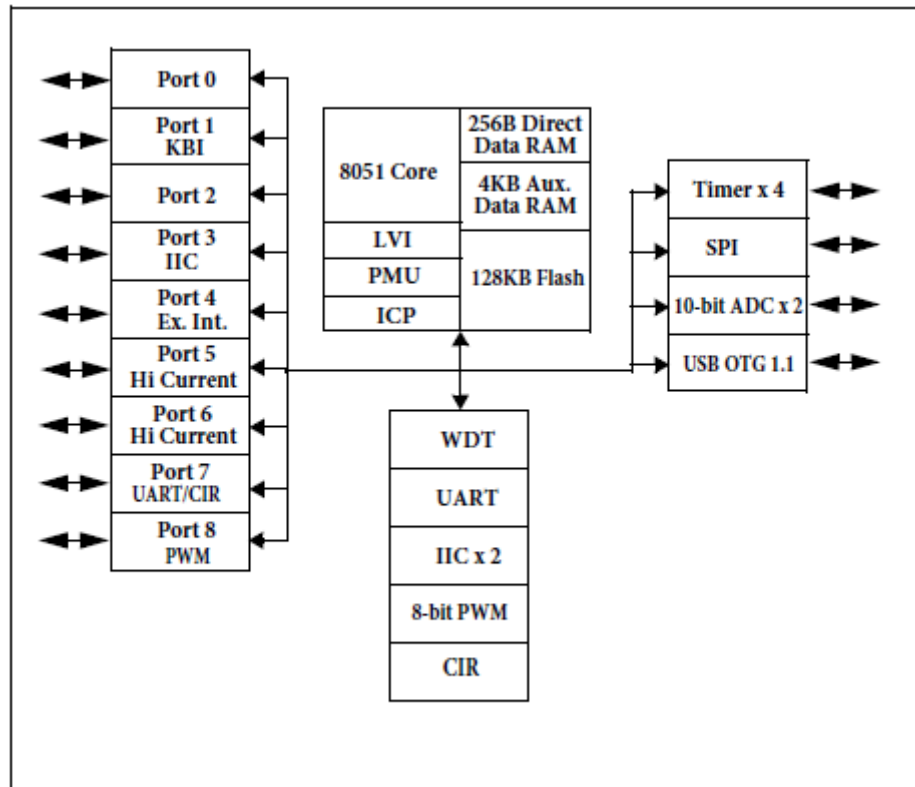


Figure 21: Block Diagram

12. OPS - OPEN PLUGGABLE SPECIFICATION(OPTIONAL)

General Description

The OPS involves the integration concept of a Pluggable Module into the display panel thru a single and standard interfacing based on the 80 pin JAE plug and receptacle connectors. The power supply to the Pluggable Module together with the defined feature interfaces are being routed through this set of connectors to provide a functional system level computing solution for digital signage. The Pluggable Module consists of a computing board (e.g., EPIC size board or smaller) in a wrapper chassis. The JAE connector enables plug and unplug mechanism between the Pluggable Module and the docking board inside the display panel.

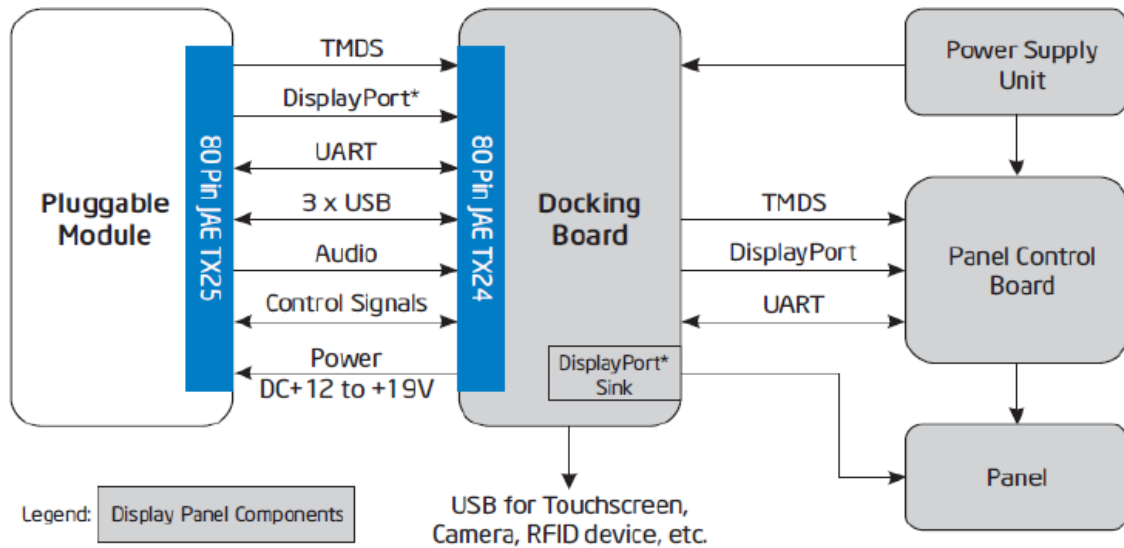


Figure 22: Functional Block Diagram

The connector used for the Pluggable Module and the docking board interconnect is based on the JAE TX24/TX25 family of plug and receptacle connectors. The JAE connector pins are capable of supporting up to a maximum current of 1A. For details refer to the JAE connector datasheet or contact a JAE representative. The 80-pin right angle blind mate plug connector (p/n: TX25-80P-LT-H1E) and its receptacle (p/n: TX24-80R-LT-H1E) provide interfacing for the following features:

Power: DC IN +12V~+19V @ 8A max

Display Interface: DVI-D/TMDS and DisplayPort

Audio: Left and Right Channel

USB: 3*USB 2.0 (when USB3.0 is not used) or 2*USB 2.0 and 1*USB 3.0

UART: Serial communication (Tx and Rx only)

Control Signals: Pluggable Module Power Status, Power ON via display panel, Pluggable Board Detect, Consumer Electronics Control (CEC), and System Fan Control.

Pin Assignment

Pin No.	Signal	Description	I/O
40	+12V**+19V	Power	-
39	+12V**+19V	Power	-
38	+12V**+19V	Power	-
37	+12V**+19V	Power	-
36	+12V**+19V	Power	-
35	+12V**+19V	Power	-
34	+12V**+19V	Power	-
33	+12V**+19V	Power	-
32	GND	Ground	-
31	DVI_HPD	DVI-D	IN
30	DVI_DDC_CLK	DVI-D	I/O
29	DVI_DDC_DATA	DVI-D	I/O
28	GND	Ground	-
27	TMD52+	DVI-D	OUT
26	TMD52-	DVI-D	OUT
25	GND	Ground	-
24	TMD51+	DVI-D	OUT
23	TMD51-	DVI-D	OUT
22	GND	Ground	-
21	TMD50+	DVI-D	OUT
20	TMD50-	DVI-D	OUT
19	GND	Ground	-
18	TMD5_CLK+	DVI-D	OUT
17	TMD5_CLK-	DVI-D	OUT
16	GND	Ground	-
15	DDP_HPD	DisplayPort	IN
14	DDP_AUXP	DisplayPort	I/O
13	DDP_AUXN	DisplayPort	I/O
12	GND	Ground	-
11	DDP_0P	DisplayPort	OUT
10	DDP_0N	DisplayPort	OUT
9	GND	Ground	-
8	DDP_1P	DisplayPort	OUT
7	DDP_1N	DisplayPort	OUT
6	GND	Ground	-
5	DDP_2P	DisplayPort	OUT
4	DDP_2N	DisplayPort	OUT
3	GND	Ground	-
2	DDP_3P	DisplayPort	OUT
1	DDP_3N	DisplayPort	OUT
80	GND	Ground	-
79	GND	Ground	-
78	GND	Ground	-
77	GND	Ground	-
76	GND	Ground	-
75	GND	Ground	-
74	PWR_STATUS	PowerGood	OUT (OC)
73	PS_ON#	Pluggable Signal ON	IN
72	PB_DET	Pluggable Board Detect	OUT
71	CEC	Consumer Electronic Control	I/O
70	AZ_LINEOUT_R	Audio-Rch	OUT
69	AZ_LINEOUT_L	Audio-Lch	OUT
68	GND	Ground	-
67	USB_PP0	USB	I/O
66	USB_PN0	USB	I/O
65	GND	Ground	-
64	USB_PP1	USB	I/O
63	USB_PN1	USB	I/O
62	GND	Ground	-
61	USB_PP2	USB	I/O
60	USB_PN2	USB	I/O
59	GND	Ground	-
58	StdA_SSTX+	USB3.0	OUT
57	StdA_SSTX-	USB3.0	OUT
56	GND	Ground	-
55	StdA_SSRX+	USB3.0	IN
54	StdA_SSRX-	USB3.0	IN
53	GND	Ground	-
52	UART_TXD	UART 3.3V	OUT
51	UART_RXD	UART 3.3V	IN
50	SYS_FAN	System Fan Control	OUT
49	RSVD	Reserved pins	-
48	RSVD	Reserved pins	-
47	RSVD	Reserved pins	-
46	RSVD	Reserved pins	-
45	RSVD	Reserved pins	-
44	RSVD	Reserved pins	-
43	RSVD	Reserved pins	-
42	RSVD	Reserved pins	-
41	RSVD	Reserved pins	-

Note 1: The I/O column definition is in reference to the pluggable board

Note 2: OC= Open Collector

Table 28: Pin Assignment

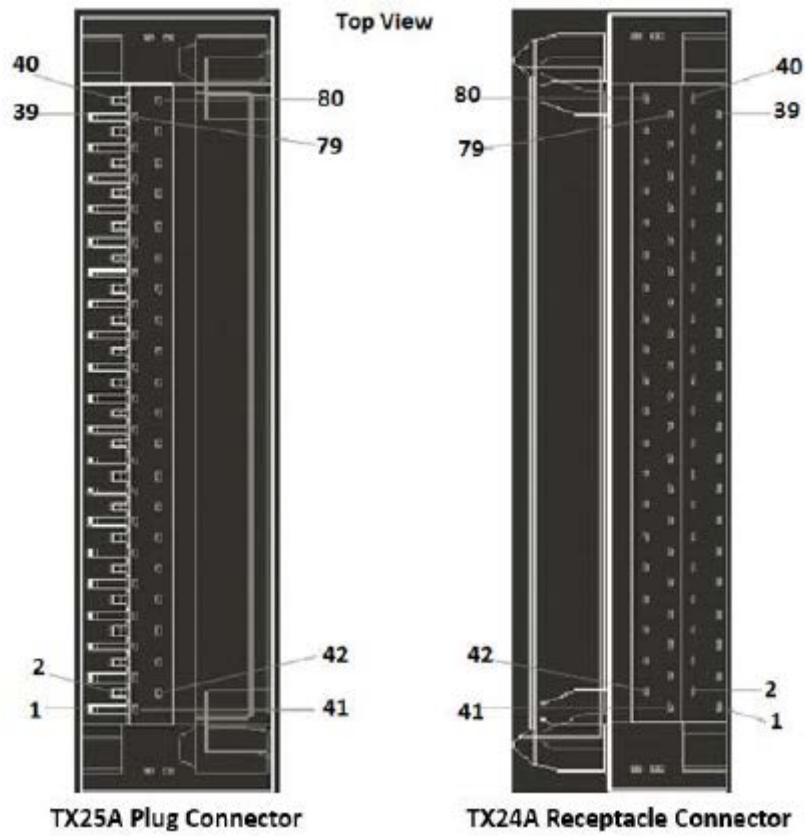


Figure 23: Compatible OPS Connector Pin Layout

13. TUNER (OPTIONAL)

M88TS2022 SATELLITE TUNER

Features and General Description

Features

- Single-chip tuner
- Compliant with DVB-S2 and ABS-S standards
- Support QPSK, 8PSK and 16APSK
- Direct-conversion from L-band to baseband
- Symbol rate: 1 to 45 Msymbol/s
- Integrated VCOs and PLL, with on-chip inductors, varactors and loop filter
- Integrated baseband filters: 4 MHz to 40 MHz bandwidth
- Integrated RF AGC for optimal performance
- Integrated baseband DC offset cancellation (patent-pending) removes external loop filters
- Excellent immunity to strong adjacent undesired channels
- Integrated clock driver provides auxiliary divided clock output for other devices
- Selectable RF bypass
- Support sleep mode
- 2-wire serial bus with 3.3 V compatible logic levels
- Power supply: +3.3 V
- 28-pin QFN (Quad Flat No-lead) package
- RoHS compliant

Applications

- Digital satellite receiver front-end for DVB-S2 and ABS-S applications

General Description

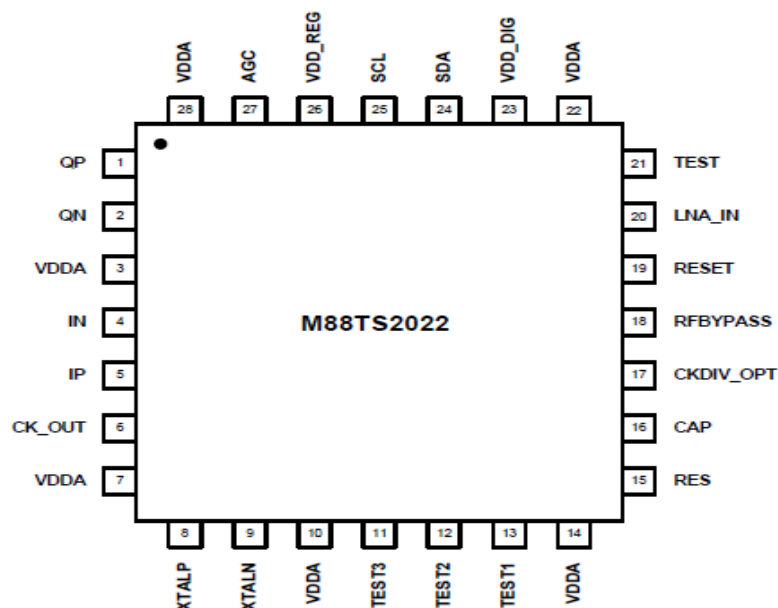
The M88TS2022 is a single-chip, direct-conversion tuner for digital satellite receiver applications. It offers the industry's most integrated solution to a satellite tuner function, simplifying the front-end designs. The device also provides an RF bypass output for driving a second tuner module.

This device incorporates the following functional blocks on a single chip: an LNA, quadrature down-converting mixers, a low phase noise and fast locking frequency synthesizer with on-chip loop filters, a DC offset cancellation loop with integrated loop filters, self-calibrated programmable baseband channel filters, an integrated RF AGC loop, and crystal oscillators with an integrated auxiliary clock output.

As a result of integrating all these blocks, the M88TS2022 has the least number of pins compared with other conventional solutions, and requires the least external components. In typical applications, the M88TS2022 requires only one crystal, one bypass capacitor, one matching network, and a few external resistors. The device also has the industry's smallest latency, as it uses a fast locking PLL and a fast settling DC offset cancellation architecture.

The M88TS2022 can be configured via a 2-wire serial bus. The chip is available in a 28-pin QFN package.

Pin Assignment



Absolute Maximum Ratings and Recommended Operating Conditions

Absolute Maximum Ratings

Symbol	Parameter	Min.	Max.	Unit	Notes
VDDA	Analog power supply	-0.6	5	V	
VDD_DIG	Digital power supply	-0.6	5	V	
V _{2-wire}	Voltage on 2-wire bus pins	-0.6	5	V	
V _{IN}	Voltage on other input pins	-0.6	2.5	V	
V _{OUT}	Output voltage	-0.6	VDDA + 0.5	V	
T _{STG}	Storage temperature	-55	150	°C	
T _{OP}	Operating ambient temperature	0	70	°C	
Note: Stresses above the Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended period may affect device reliability.					

Recommended Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
VDDA, VDD_DIG	Analog power supply	3.0	3.3	3.6	V	With respect to VSS
T _{OP}	Operating ambient temperature	0		70	°C	
Note: Device functionality is not guaranteed at any conditions beyond the recommended operating conditions.						

14. DEMODULATOR STAGE (OPTIONAL)

A.MSB1246 DVB-T2

Features

■ DVB-T2

- Compliant with ETSI EN 302 755 v 1.3.1
- Supports T2-base and T2-Lite profile
- Supports 1.7, 5, 6, 7, 8MHz bandwidth
- Supports all guard intervals (1/128 to 1/4)
- Supports all FFT modes from 1K to 32K
- Supports all long and short block code rates (1/2, 3/5, 2/3, 3/4, 4/5, 5/6 and 1/3, 2/5 specific to T2-Lite)
- Supports all constellations (QPSK, 16-QAM, 64-QAM, 256-QAM)
- Supports transmit diversity (MISO)
- Supports all scattered pilot patterns (PP1 to PP8)
- Supports rotated and non-rotated constellations
- Supports single and multiple PLPs
- Compliant with Nordig 2.2.2, D-Book 7.0 and Ghana test suite v1.1
- Automatic co-channel and adjacent channel interference suppression
- All digital demodulation and timing recovery loops for tracking frequency and clock offset
- Impulse-Noise suppression
- Advanced performance for SFN networks

■ DVB-S2/S

- Compliant with DVB-S2 (ETSI EN 302 307)
- Compliant with DVB-S (ETSI EN 300 421)
- DVB-S2:
 - Data Rate: 1-45 Msps
 - Constellations: QPSK and 8PSK
 - Code Rates: 1/2, 3/5, 2/3, 3/4, 4/5, 5/6, 8/9 and 9/10
 - Roll-off factors for pulse shaping: 0.2, 0.25, and 0.35
- DVB-S:
 - Data Rate: 1-45 Msps
 - Code Rates: 1/2, 2/3, 3/4, 5/6, 7/8
- Directly interfaces with tuner for easy implementation
- Integrated dual A/D converters
- Carrier frequency acquisition range: $\pm 5\text{MHz}$
- Fast automatic blind scan of symbol rates and carrier frequencies
- Equalizer compensates for channel impairment
- DiSEqC™ 2.0 compatible with LNB controller

■ DVB-T

- Compliant with ETSI EN 300 744
- Supports all guard intervals (1/32 to 1/4)
- Supports 2K and 8K FFT modes
- Supports all code rates (1/2, 2/3, 3/4, 5/6, 7/8)
- Supports all constellations (QPSK, 16-QAM, 64-QAM)
- Automatic co-channel and adjacent channel interference suppression
- All digital demodulation and timing recovery loops for tracking frequency and clock offset
- Impulse-Noise suppression
- Advanced performance for SFN networks

■ DVB-C

- Compliant with ETSI EN 300 429
- Supports symbol rate from 1 to 7.2 MHz
- Automatic symbol rate detection and QAM-mode detection
- All digital demodulation and timing recovery loops for tracking frequency and clock offset

- Automatic co-channel and adjacent channel interference suppression
- Impulse-Noise suppression
- All digital demodulation and timing recovery loops for tracking frequency and clock offset
- Novel carrier recovery algorithms for tracking and compensating large phase noises
- Integrated FEC decoders for near Shannon limit performances

■ Miscellaneous

- For DVB-T2/T/C, accepts IF, low IF inputs
- For DVB-S2/S, accepts ZIF inputs
- Integrated signal quality and BER monitors
- Configurable parallel/serial MPEG-2 transport stream interface
- Fast channel acquisition and auto-scan time
- Clock generation from a single crystal
- On chip MCU to reduce host control overhead
- Supports I2C interface with bypass mode
- 48-pin LQFP package

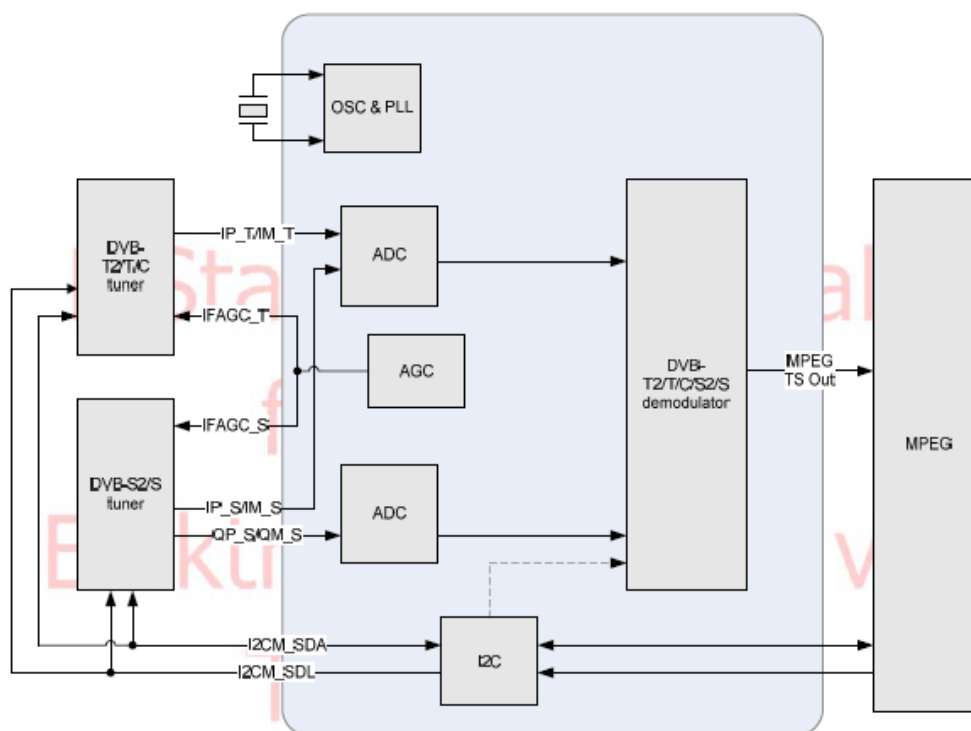
General Description

The MSB1246 is a single chip demodulator supporting DVB-T2, DVB-T, DVB-C, DVB-S2 and DVB-S standards. The device integrates a house keeping microcontroller that takes care of all real time and algorithmic tasks simplifying the host control interface.

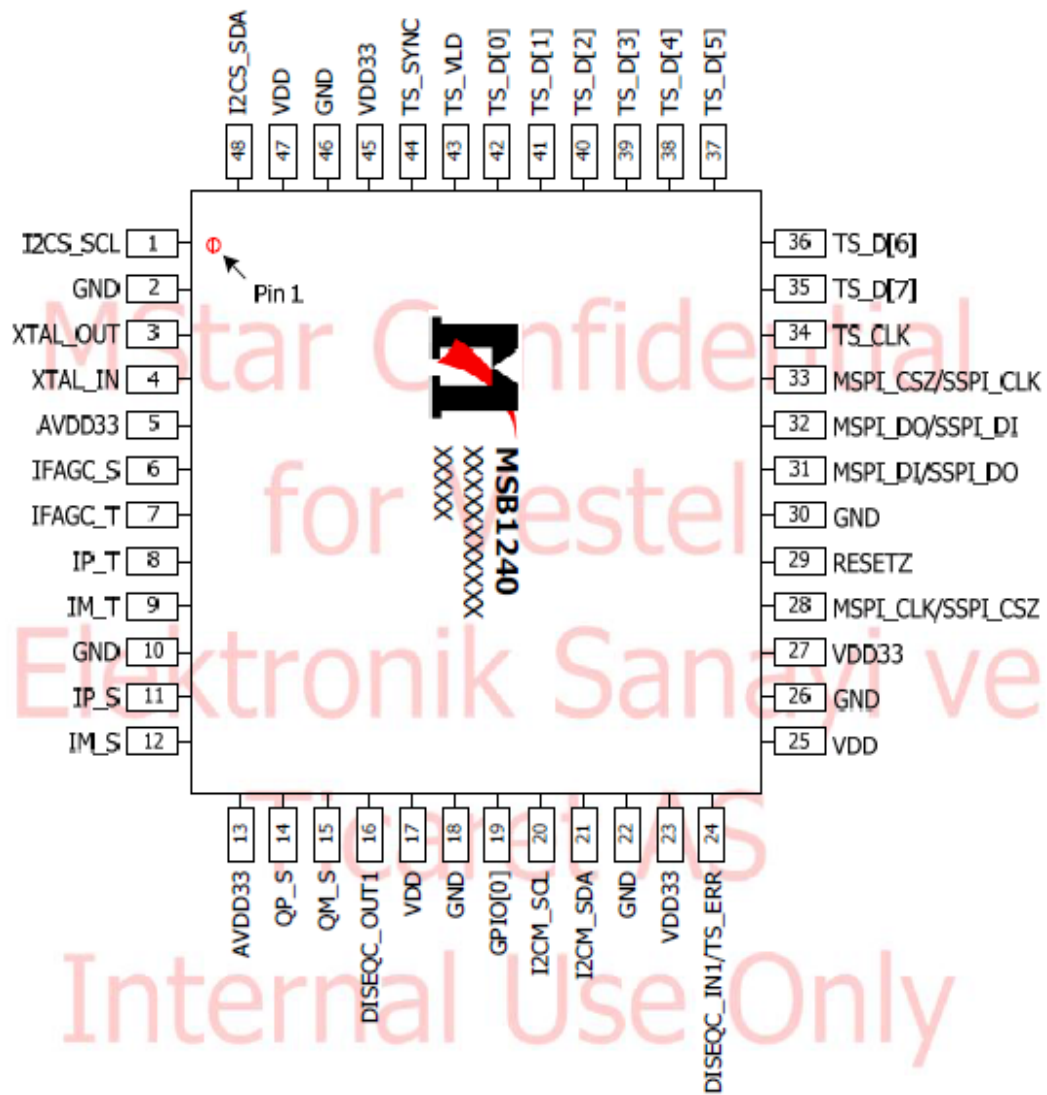
For DVB-T2/T/C, the MSB1246 front end can accept tuners that provide IF or low IF output. For DVB-S2/S, the MSB1246 front end can accept tuners that provide zero-IF output. A high rejection channel filter has been included easing the channel filtering requirement of the tuner whilst still meeting the stringent requirements for adjacent channel interference. The MSB1246 may be clocked directly using a crystal, typically 24MHz.

The MSB1246 is capable of blind acquisition of DVB-T/T2, DVB-C and DVB-S2/S signals. All parameters may be detected in this mode enabling fast and accurate auto scanning. Its frequency recovery circuit is able to compensate for all typical tuner and broadcast frequency errors.

Block Diagram



Pinning



Absolute Maximum Ratings and Recommended Operating Conditions

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units
3.3V Supply Voltages	V_{VDD_33}	3.14	3.3	3.46	V
1.15V Supply Voltages	V_{VDD_115}	1.09	1.15	1.21	V
Ambient Operating Temperature	T_A	0		70	°C
Junction Temperature	T_J			125	°C

Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Units
3.3V Supply Voltages	V_{VDD_33}		3.6	V
1.15V Supply Voltages	V_{VDD_115}		1.26	V
Input Voltage (5V tolerant inputs)	$V_{IN5Vtol}$		5.0	V
Input Voltage (non 5V tolerant inputs)	V_{IN}		V_{VDD_33}	V
Storage Temperature	T_{STG}	-40	150	°C

Note: Stresses above those listed in Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and does not imply functional operation of the device. Exposure to absolute maximum ratings for extended periods may affect device reliability.

15. LNB SUPPLY AND CONTROL IC (OPTIONAL)

TPS65233

General Description

Designed for analog and digital satellite receivers, the TPS65233 is a monolithic voltage regulator with I2C interface, specifically to provide the 13-V/18-V power supply and the 22-kHz tone signaling to the LNB downconverter in the antenna dish or to the multi-switch box. It offers a complete solution with very low component count, low power dissipation together with simple design and I2C standard interfacing. TPS65233 features high power efficiency. The boost converter integrates a 120-mΩ power MOSFET running at 500-kHz switching frequency. Drop out voltage at the linear regulator is 0.8 V to minimize power loss. TPS65233 provides multiple ways to generate the 22-kHz signal. Integrated linear regulator with push-pull output stage generates clean 22-kHz tone signal superimposed at the output even at zero loading. Current limit of linear regulator can be programmed by external resistor with $\pm 10\%$ accuracy. Full range of diagnostic read by I2C is available for system monitoring.

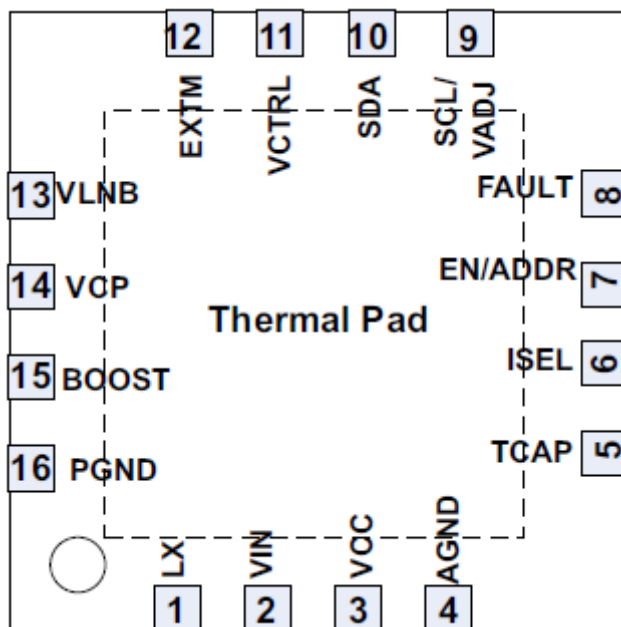
Features

- Complete Integration Solution for LNB and I²C
- DiSEqC 1.x Compatible
- Supports 5-V and 12-V Power Bus
- Up to 1000-mA Accurate Output Current Limit Adjustable by External Resistor and I²C
- Boost Converter With Low R_{dson} Internal Power Switch
- Dedicated Enable Pin for Non-I²C Application
- Low Noise, Low Drop Output With Push-Pull Output Stage
- Built-In Accurate 22-kHz Tone Generator or External Pin
- Adjustable Soft-Start and 13-V/18-V Voltage Transition Time
- Compliant with main satellite receiver systems Specifications
- LNB Short Circuit Dynamic Protection
- Diagnostics for Output Voltage Level, Input Supply UVLO, and DiSEqC Tone Output
- Cable Disconnect Diagnostic
- Available in a 16-Pin QFN 3-mm x 3-mm (RTE) Package

APPLICATIONS

- Set Top Box Satellite Receiver
- TV Satellite Receiver
- PC Card Satellite Receiver

Pinouts



16. BQ32000 RTC REAL-TIME CLOCK (OPTIONAL)

General Description

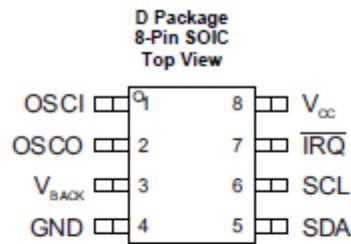
The bq32000 device is a compatible replacement for industry standard real-time clocks. The bq32000 features an automatic backup supply with integrated trickle charger. The backup supply can be implemented using a capacitor or non-rechargeable battery. The bq32000 has a programmable calibration adjustment from -63 ppm to +126 ppm. The bq32000 registers include an OF(oscillator fail) flag indicating the status of the RTC oscillator, as well as a STOP bit that allows the host processor to disable the oscillator. The time registers are normally updated once per second, and all the registers are updated at the same time to prevent a timekeeping glitch. The bq32000 includes automatic leap-year compensation.

Features

- Automatic Switchover to Backup Supply
- I²C Interface Supports Serial Clock up to 400 kHz
- Uses 32.768-kHz Crystal With -63-ppm to +126-ppm Adjustment

- Integrated Oscillator-Fail Detection
- 8-Pin SOIC Package
- -40°C to 85°C Ambient Operating Temperature

Pin Configuration and Functions



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
POWER AND GROUND			
GND	4	-	Ground
V _{BACK}	3	-	Backup device power
V _{CC}	8	-	Main device power
SERIAL INTERFACE			
SCL	6	I	I ² C serial interface clock
SDA	5	I/O	I ² C serial data
INTERRUPT			
IRQ	7	O	Configurable interrupt output. Open-drain output.
OSCILLATOR			
OSCI	1	-	Oscillator input
OSCO	2	-	Oscillator output

17. SOFTWARE UPDATE

A. MAIN SW UPDATE

In 17MB120DS project, please follow software update procedure:

1. mb120_en.bin, RomBoot.bin, PM51.bin and usb_auto_update_G6F.txt documents should be copied directly inside of a flash memory (not in a folder).
2. Insert flash memory to the TV when TV is powered off.
3. While pushing the OK button in remote control, power on and wait. TV will power-up itself.
4. If First Time Installation screen comes, it means software update procedure is successful.

B. DISPLAYPORT FW UPDATE

Please follow DP fw update procedure:

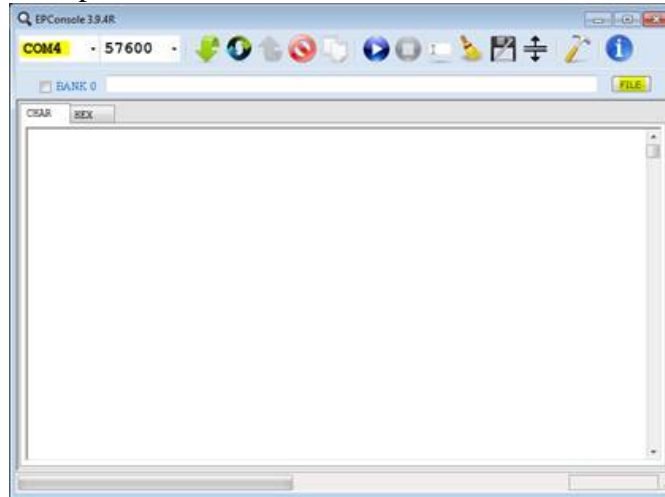
1. Connect DP source with DP input port of 17MB120DS.
2. Run McdpAuxISPTool on source.
3. Choose the correct “Driver File” and “FW File”, then click to start.
4. After update process, new version could be check with “Get FW Version” button on tool.

C. HDMI SPLITTER FW UPDATE

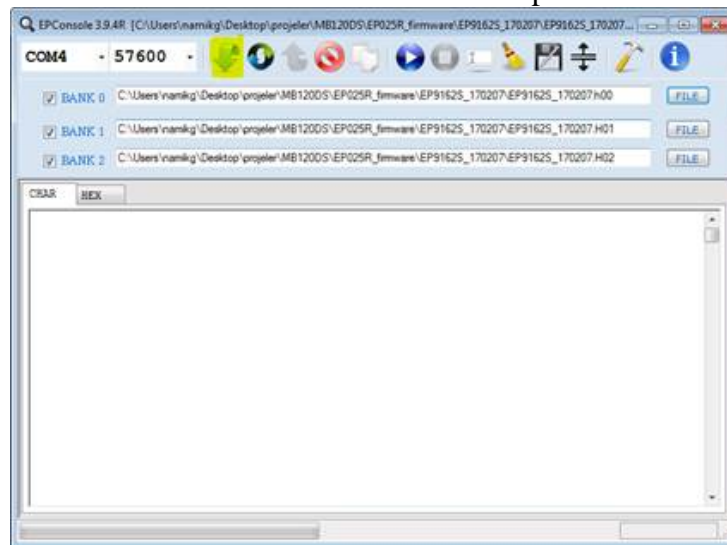
Please follow HDMI splitter fw update procedure:

1. Connect Mstar tool via RJ12 service socket with HDMI fw cable.
2. Run EPConsole program on PC after power on the MB120DS.

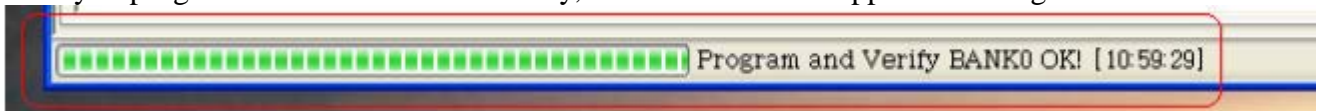
3. Select the corresponding COM port and click File to load the fw hex file.



4. Press “Program MCU “ to enter ICP mode. Then restart the DS product.



5. When you finish all of settings, press “Program MCU “ again to program the firmware.
6. When you program the firmware successfully, EP Console would appear a message of OK .



7. Finally restart the DS product.

If you see fail, please reset monitor and try program again.

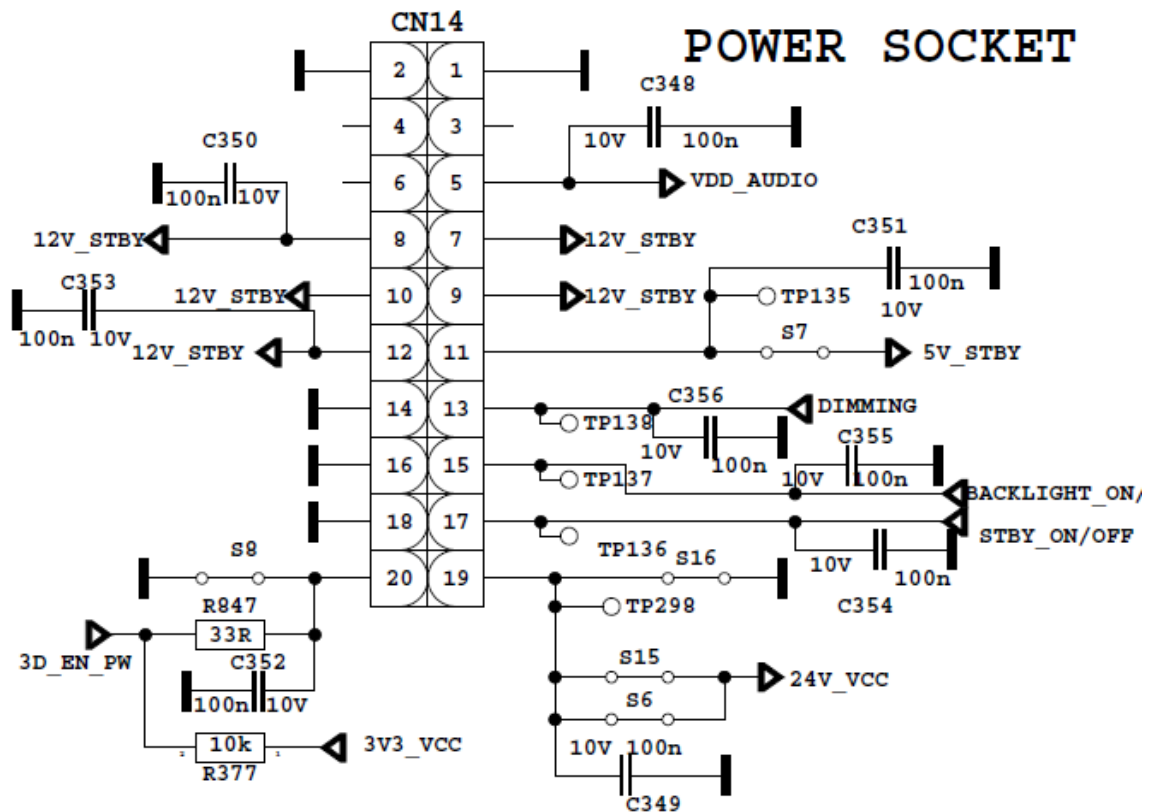
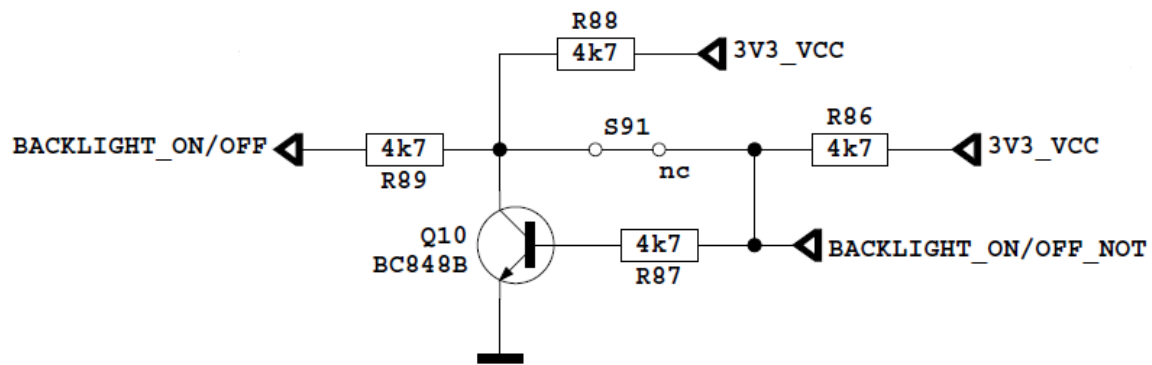
18. TROUBLESHOOTING

A. NO BACKLIGHT PROBLEM

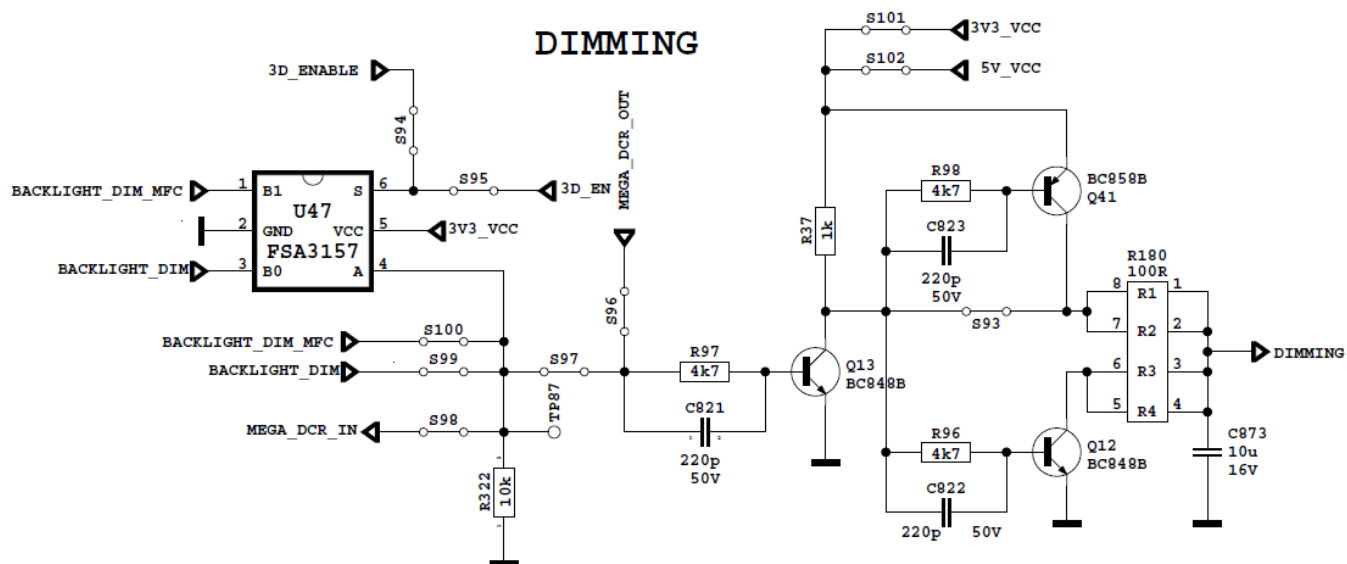
Problem: If product is working, led is normal and there is no picture and backlight on the panel.

Possible causes: Backlight pin, dimming pin, backlight supply, stby on/off pin

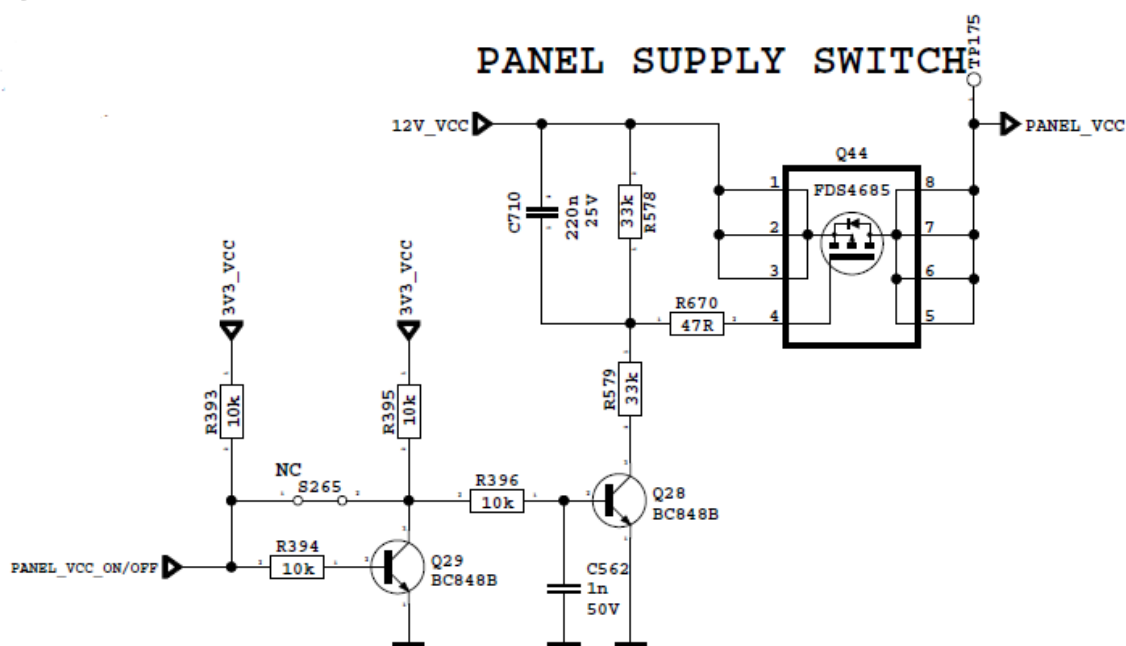
BACKLIGHT_ON/OFF pin should be high when the backlight is ON. R89 must be low when the backlight is OFF. If it is a problem, please check Q10 and the panel cables. Also it can be tested in TP137 on main board



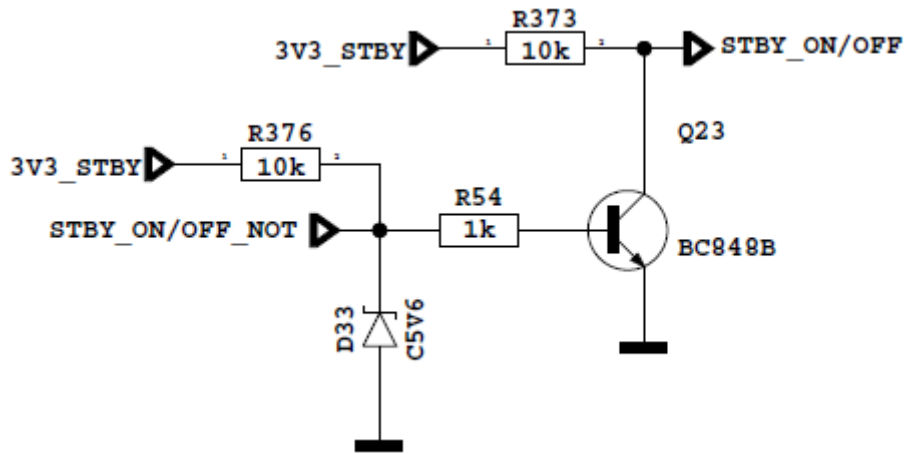
Dimming pin should be high or square wave in open position. If it is low, please check S97 for Mstar side and panel or power cables, connectors.



Backlight power supply should be in panel specs. Please check Q44, shown below; also it can be checked TP175.



STBY_ON/OFF_NOT should be low for tv on condition, please check Q23's collector.

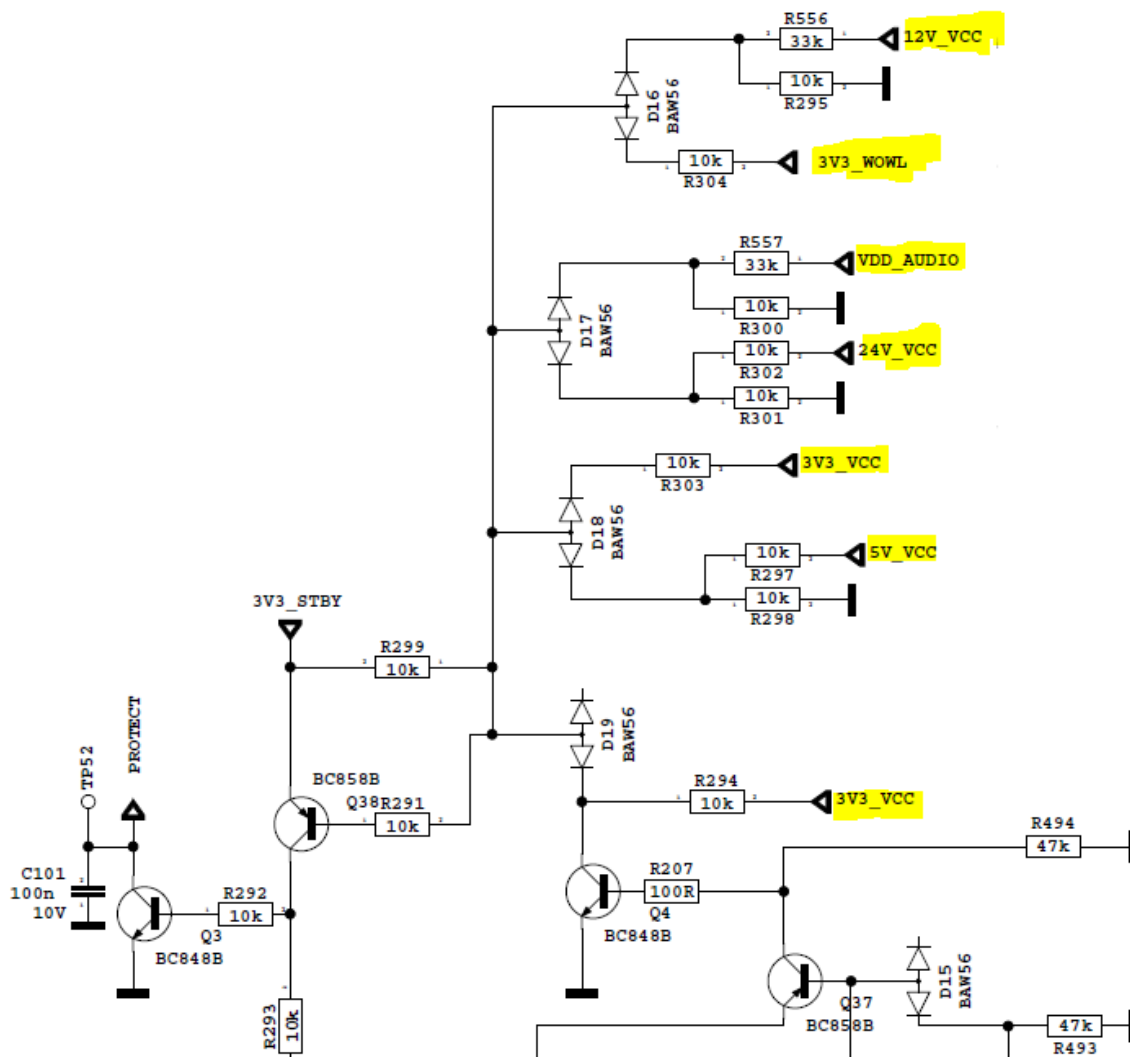


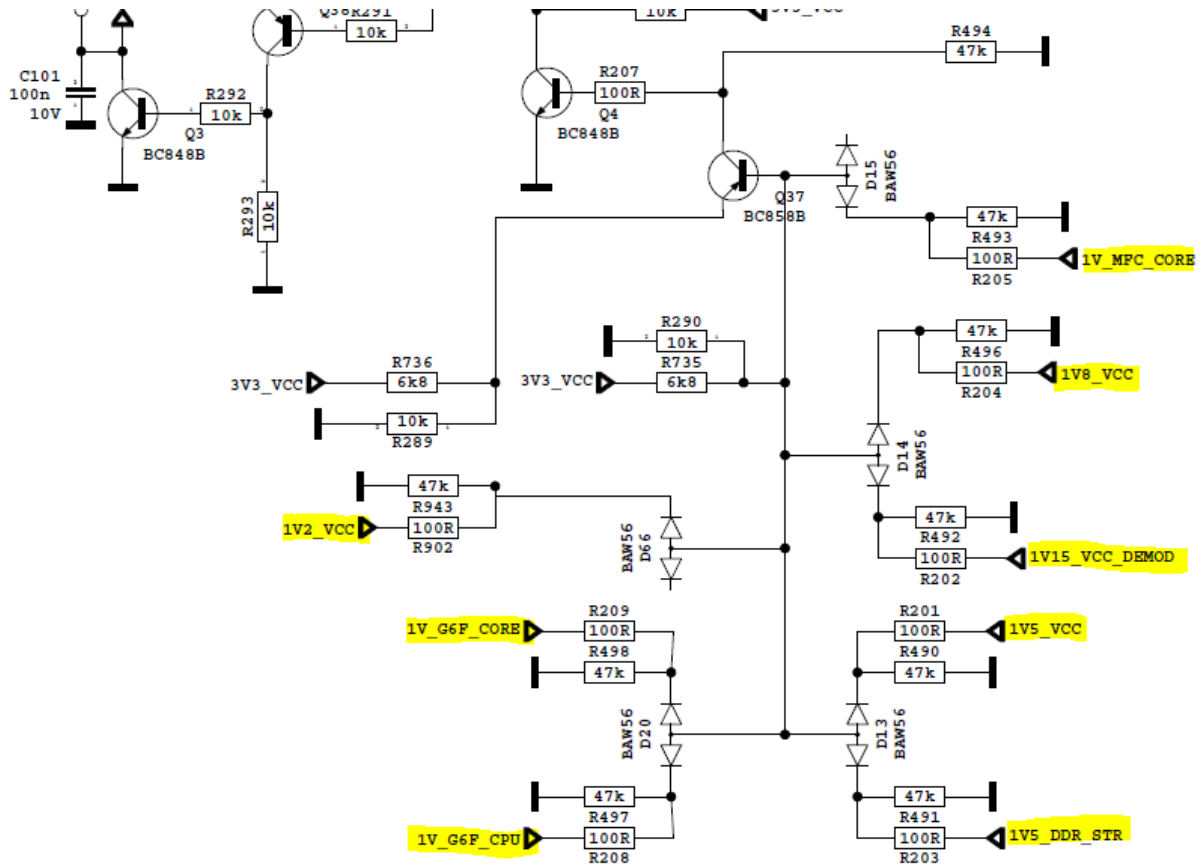
B. STAYING IN STAND-BY MODE

Problem: Staying in stand-by mode, no other operation

This problem indicates a short on Vcc voltages. Protect pin should be logic high while normal operation. When there is a short circuit protect pin will be logic low. If you detect logic low on protect pin, unplug the product set and control voltage points with a multimeter to find the shorted voltage to ground.

SHORT CCT PROTECTION

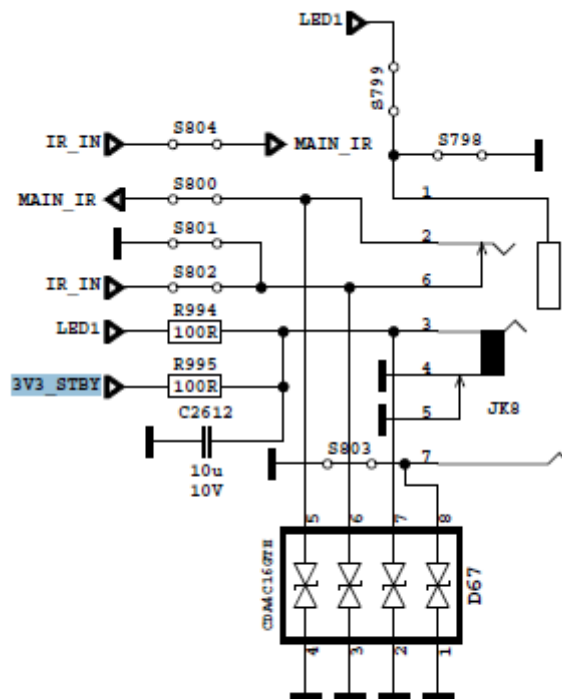




C.IR PROBLEM

Problem: Extender LED or IR not working

Check Extender LED/IR card supply on 17MB120DS chasis.

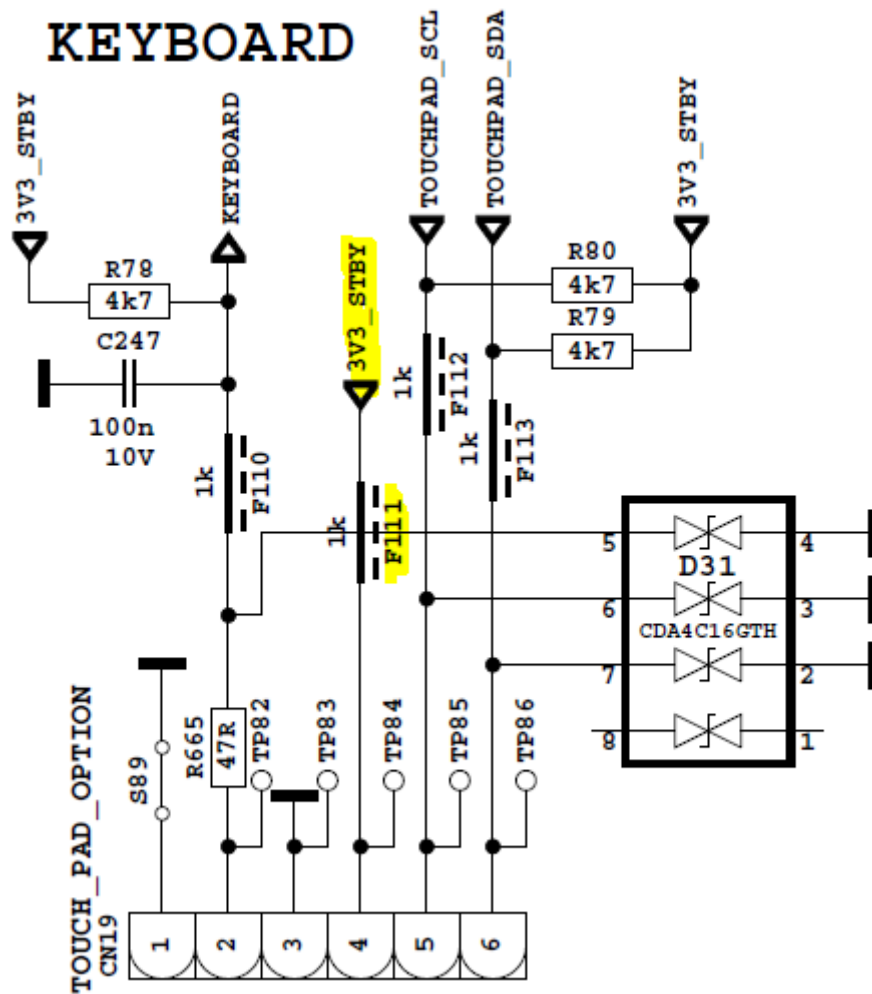


IR EXTENDER

D.KEYPAD TOUCHPAD PROBLEMS

Problem: Keypad or Touchpad is not working

Check keypad supply on MB120.

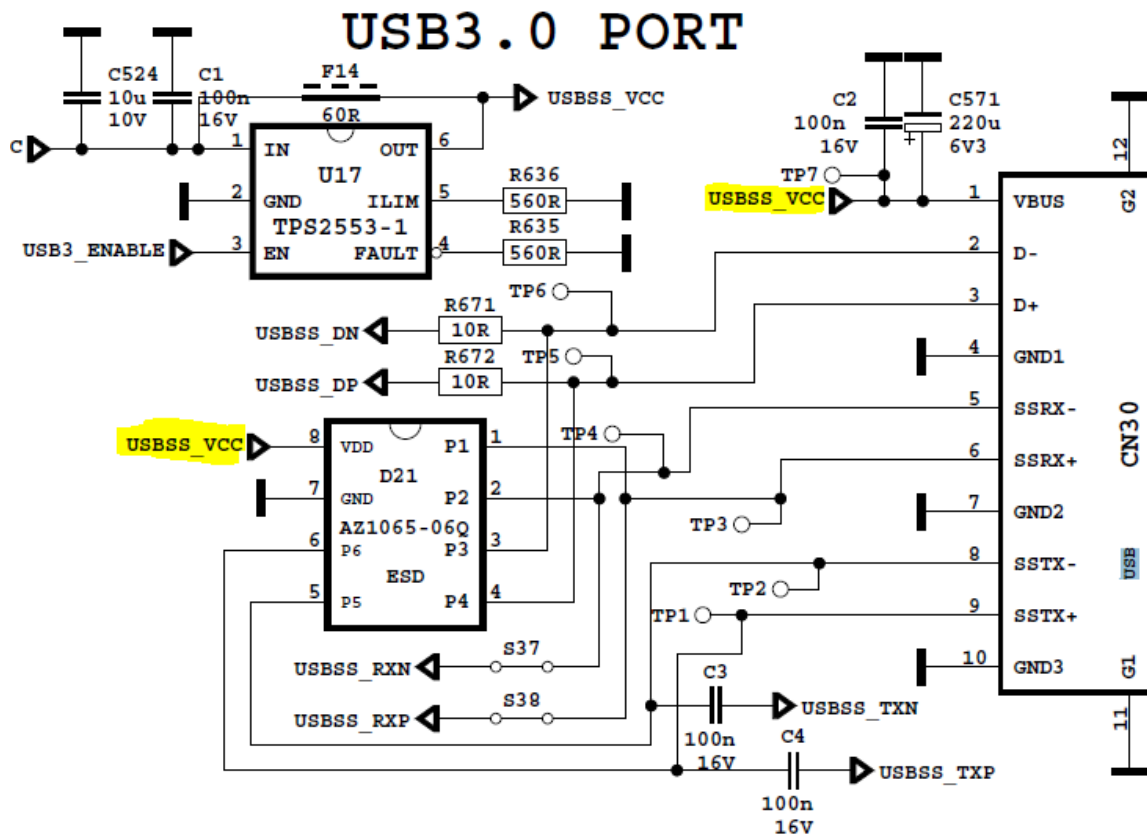


E. USB PROBLEMS

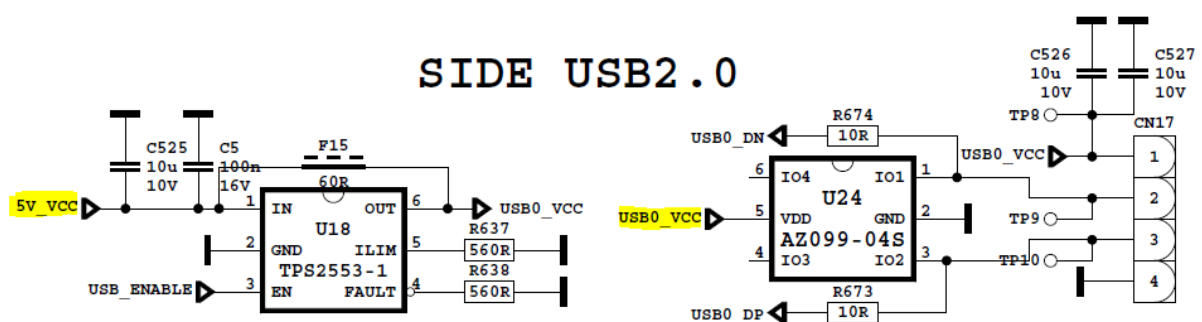
Problem: USB is not working or no USB Detection.

Check USB Supply, It should be nearly 5V. Also USB Enable should be logic high.

For USB 3.0 ports:



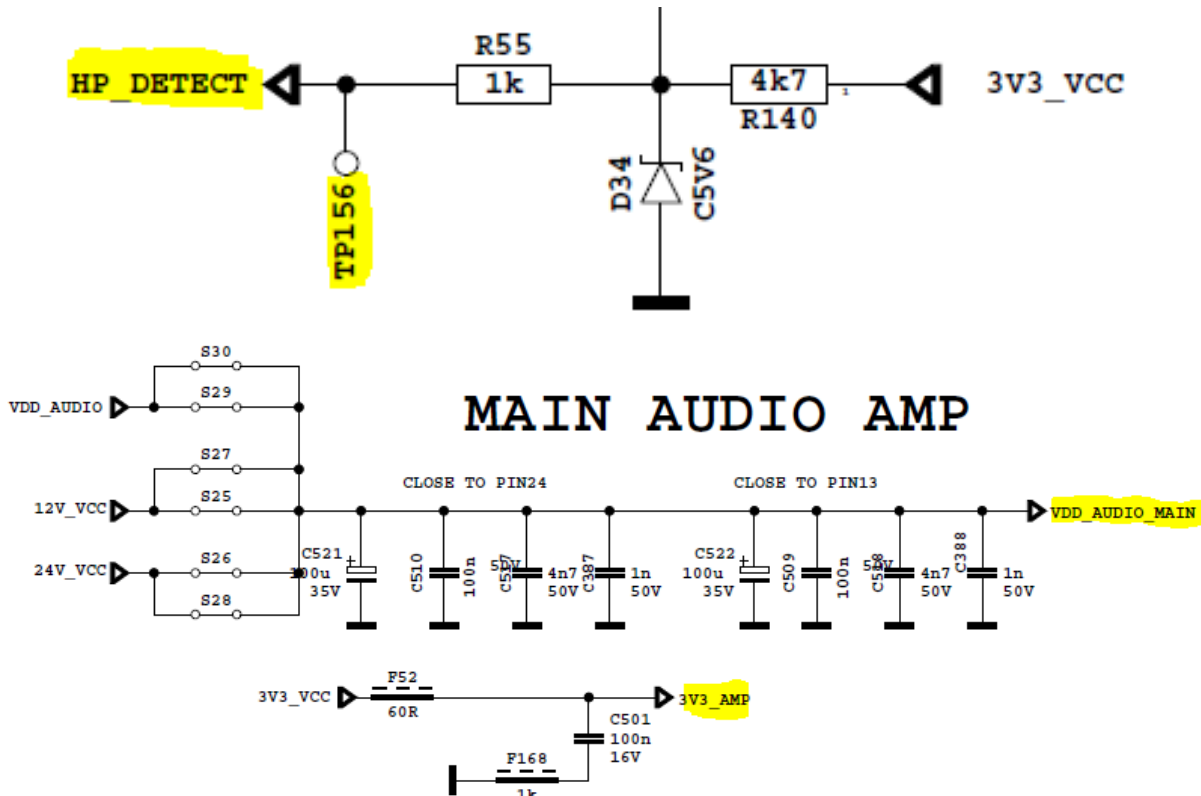
For Side USB 2.0 port:



F. NO SOUND PROBLEM

Problem: No audio at main TV speaker outputs.

Check supply voltages of 24V_VCC, VDD_AUDIO_MAIN and 3.3V_AMP with a voltage-meter. There may be a problem in headphone connector or headphone detect circuit (when headphone is connected, speakers are automatically muted). Measure voltage at HP_DETECT pin, it should be 3.3v.



G. STANDBY ON/OFF PROBLEM

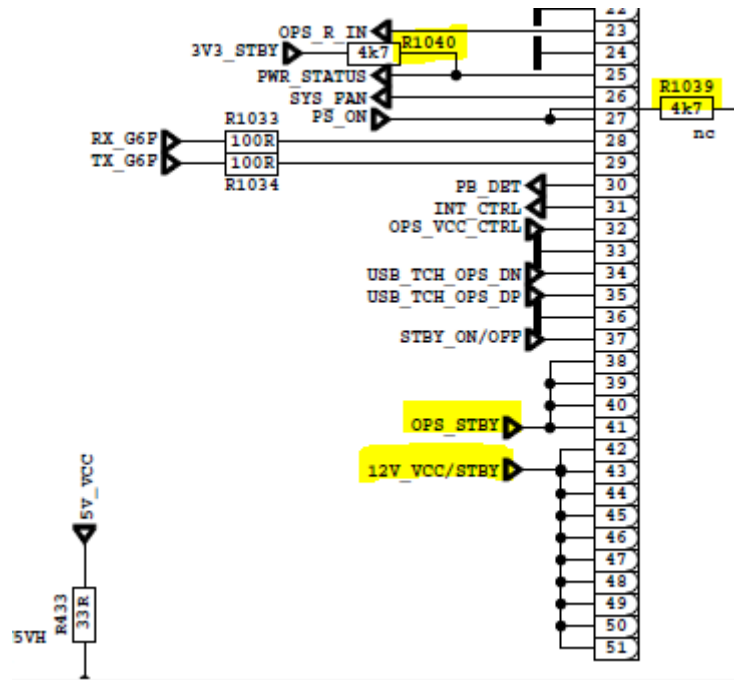
Problem: Device can not boot, TV hangs in standby mode.

There may be a problem about power supply. Check main supplies with a voltage-meter. Also there may be a problem about SW. Try to update TV with latest SW. Additionally it is good to check SW printouts via Teraterm. These printouts may give a clue about the problem. You can use RJ12 service socket for terraterm connection.

H. NO SIGNAL PROBLEM

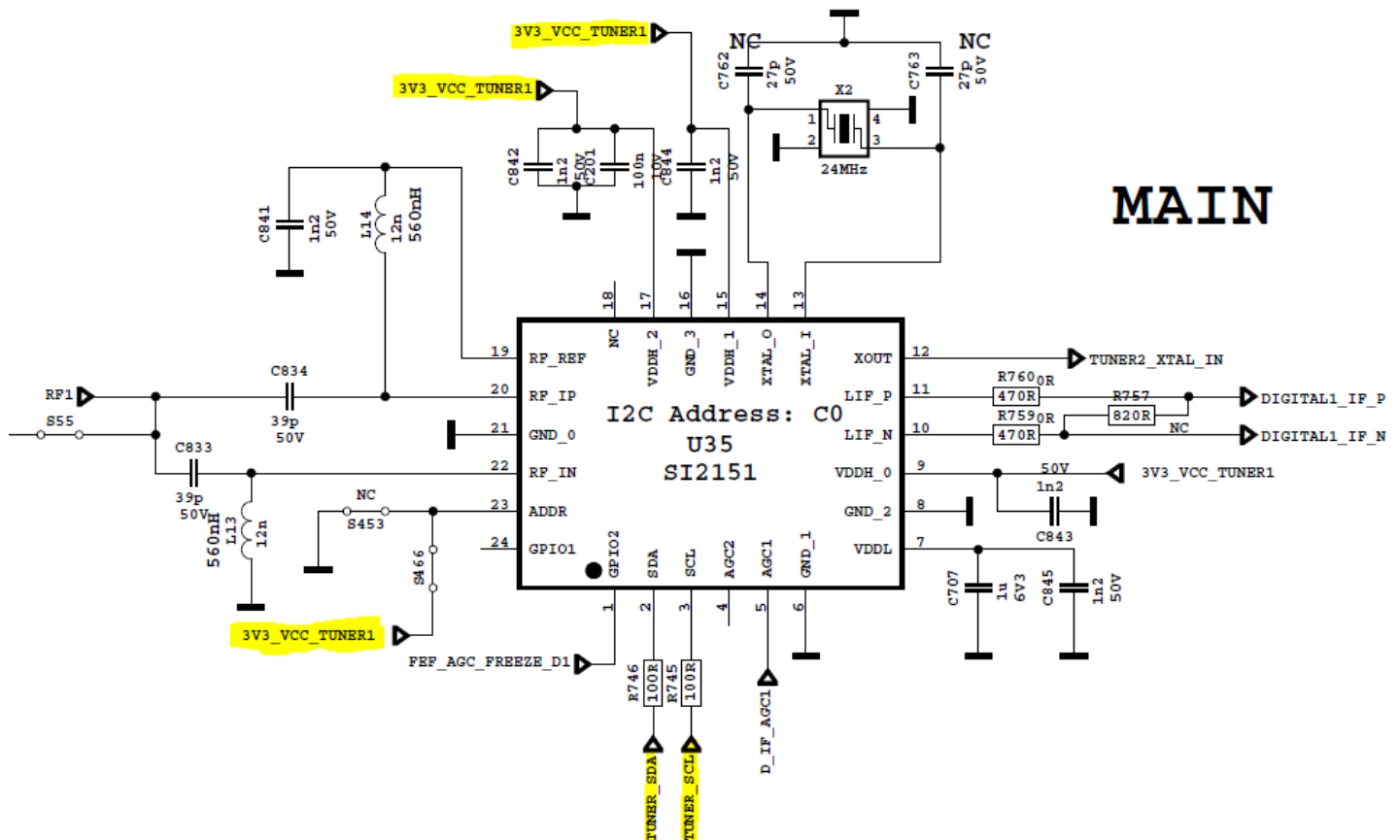
Problem: No signal in OPS mode.

Check OPS supply voltage 12V_VCC/STBY and OPS_STBY(according to power board). Check PS_ON signal(R1039) while OPS is being started. A pulse width present on the PS_ON shall be detected and responded within 200 ms to ensure successful operation. Check PWR_STATUS signal (R1040); it must be low if Pluggable board is power on state. There may be a SW problem, try to update product with latest SW.



Problem: No signal in TV mode.

Check tuner supply voltage 3V3_TUNER1 and. Check tuner options are correctly set in Service menu. Check voltage at TUNER_SCL and TUNER_SDA pin of tuner.

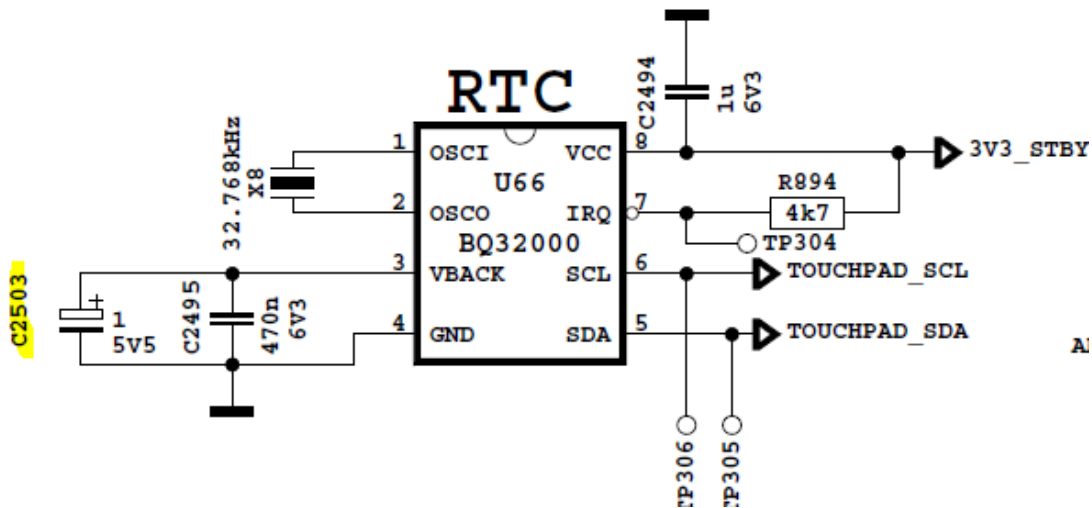


MAIN

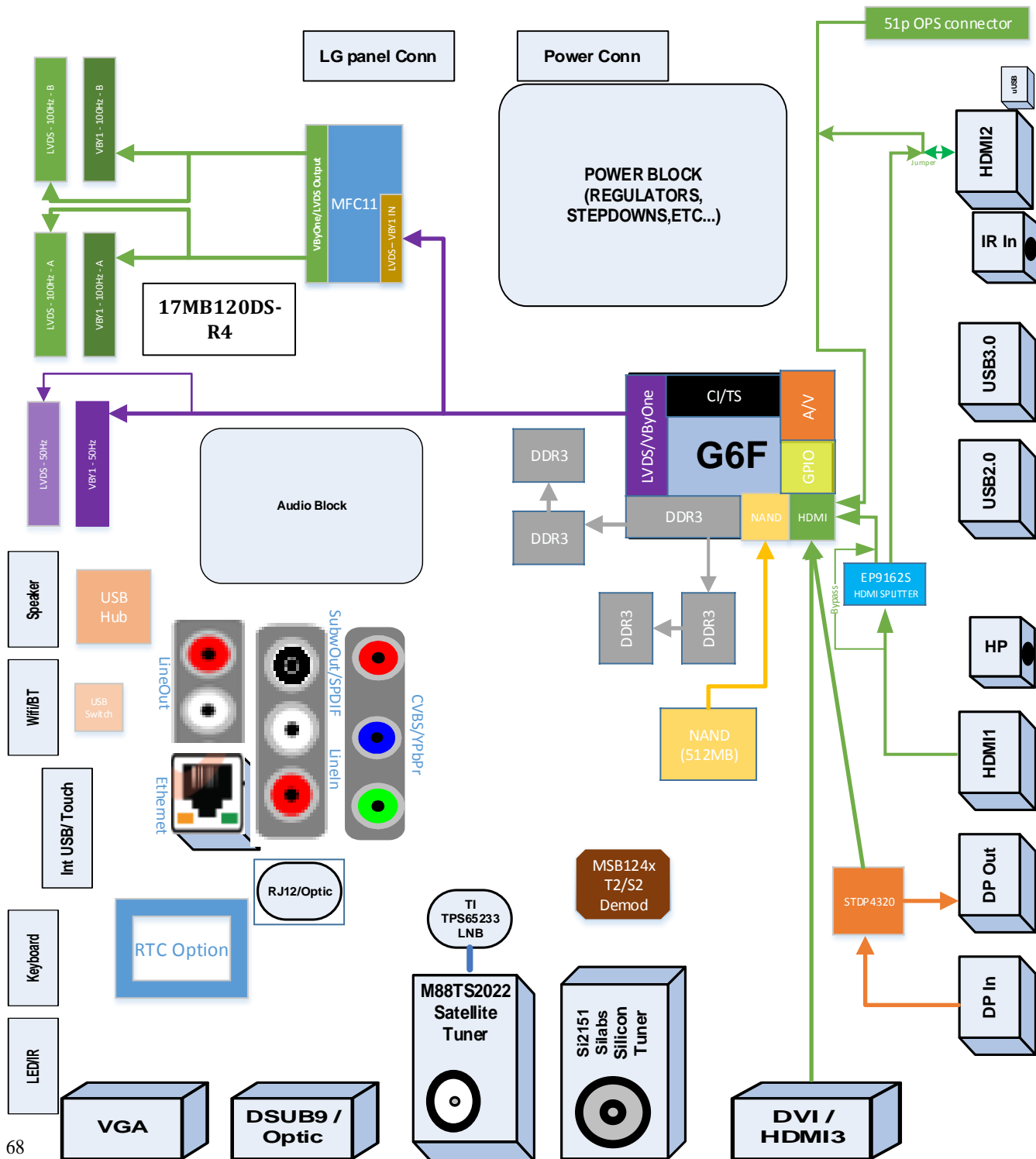
I. REAL TIME CLOCK PROBLEM

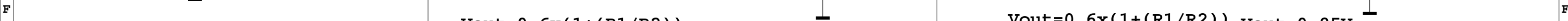
Problem: Date/Time Failure

Check RTC supply voltage 3V3_STBY. Also there may be a problem about backup supply. Please check voltage level of C2503.

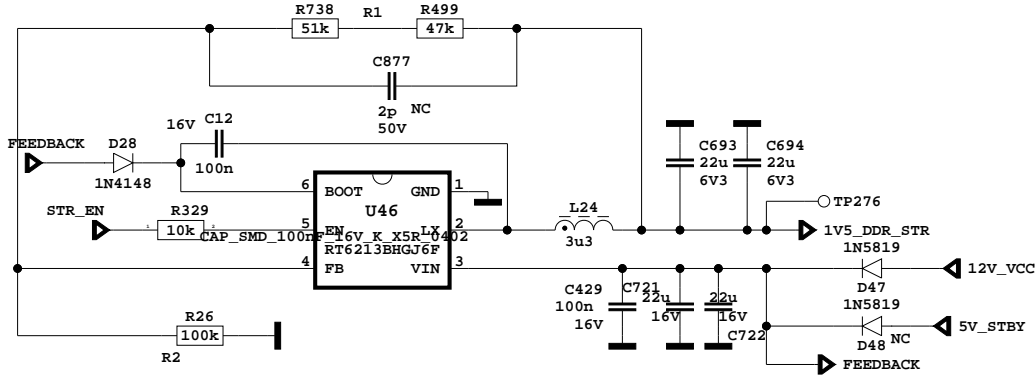


19. GENERAL BLOCK DIAGRAM





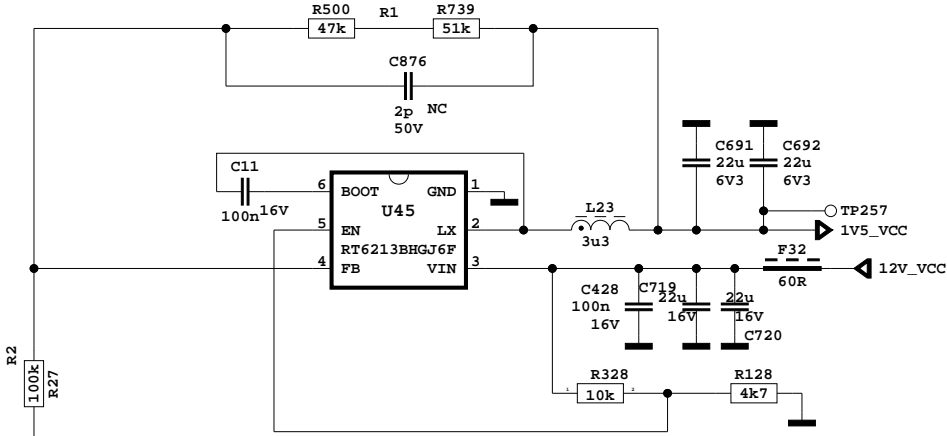
1V5_DDR_STR W/FAST POWER ON



$$V_{out} = 0.765 \times (1 + (R1/R2))$$
$$R1 = 98k \quad R2 = 100k$$

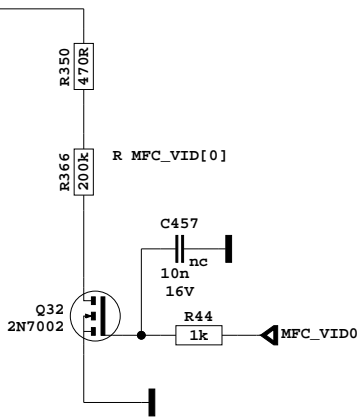
30091220
TPS562200 ADJ/2A SOT23

1V5_VCC

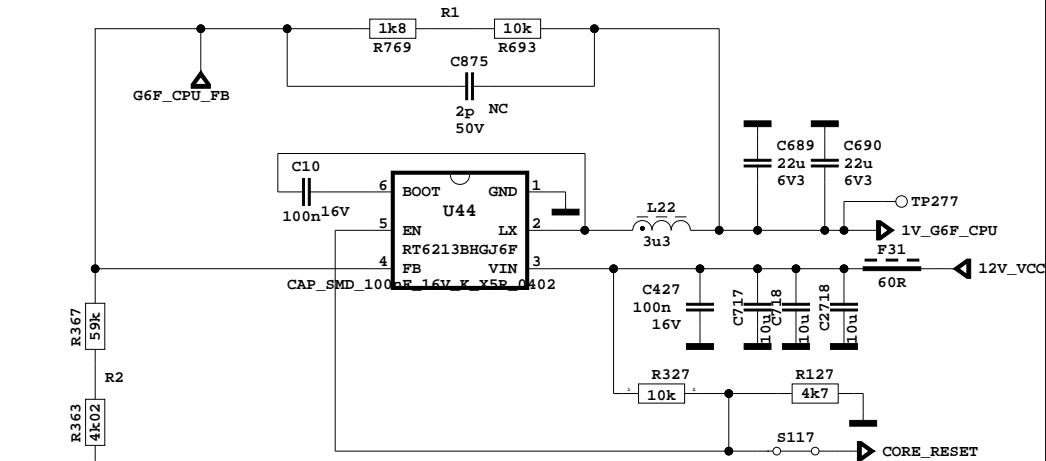


$$V_{out} = 0.765 \times (1 + (R1/R2))$$
$$R1 = 98k \quad R2 = 100k$$

30091219
TPS563200 ADJ/3A SOT23



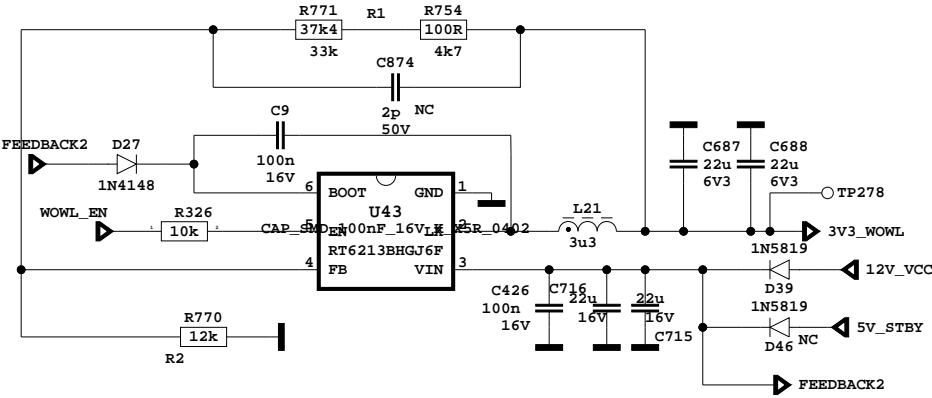
1V_G6F_CPU



$$V_{out} = 0.765 \times (1 + (R1/R2))$$
$$R1 = 11k8 \quad R2 = 63k$$

30091219
TPS563200 ADJ/3A SOT23

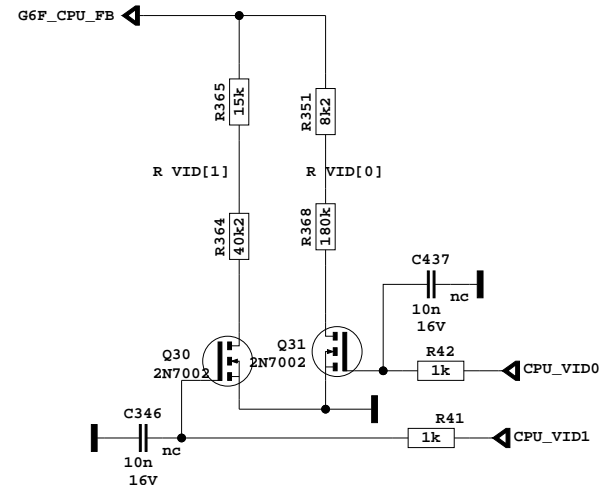
3V3_WOWL W/WOWL



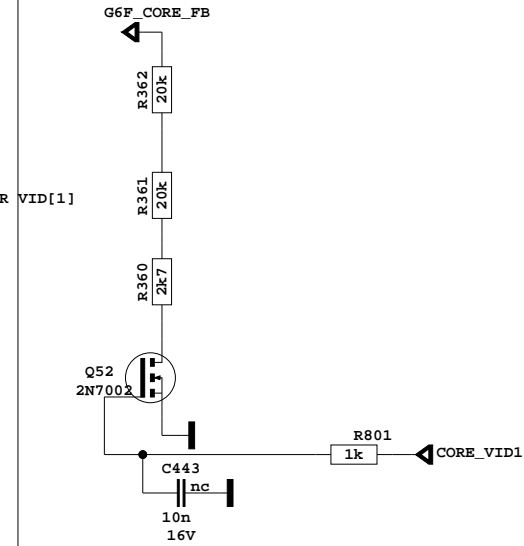
$$V_{out} = 0.765 \times (1 + (R1/R2))$$
$$R1 = 37k5 \quad R2 = 12k$$

30091220
TPS562200 ADJ/2A SOT23

MFC_VID[0]	R2	Vout
L	17k1	0,95 V
H	14k6	1,01 V



VID[0]	VID[1]	R2	Vout
L	L	63k	0,95 V
L	H	47k2	1 V
H	L	29k5	1,12 V
H	H	24k2	1,19 V



VID[0]	VID[1]	R2	Vout
L	L	17k1	0,95 V
L	H	15k	1 V
H	L	12k2	1,09 V
H	H	10k9	1,15 V

